

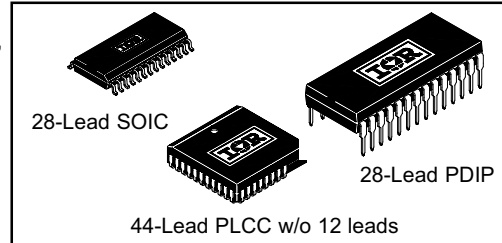
IR2136/IR21362/IR21363/IR21365/ IR21366/IR21367/IR21368 (J&S) & (PbF)

Features

- Floating channel designed for bootstrap operation
Fully operational to +600V
Tolerant to negative transient voltage - dV/dt immune
- Gate drive supply range from 10 to 20V (IR2136/IR21368),
11.5 to 20V (IR21362) or 12 to 20V (IR21363/IR21365/
IR21366/IR21367)
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent 3 half-bridge drivers
- Matched propagation delay for all channels
- Cross-conduction prevention logic
- Lowside outputs out of phase with inputs. High side
outputs out of phase (IR2136/IR21363/IR21365/
IR21366/IR21367/IR21368) or in phase
(IR21362) with inputs.
- 3.3V logic compatible
- Lower di/dt gate driver for
better noise immunity
- Externally programmable
delay for automatic fault
clear
- Also available LEAD-FREE

3-PHASE BRIDGE DRIVER

Packages

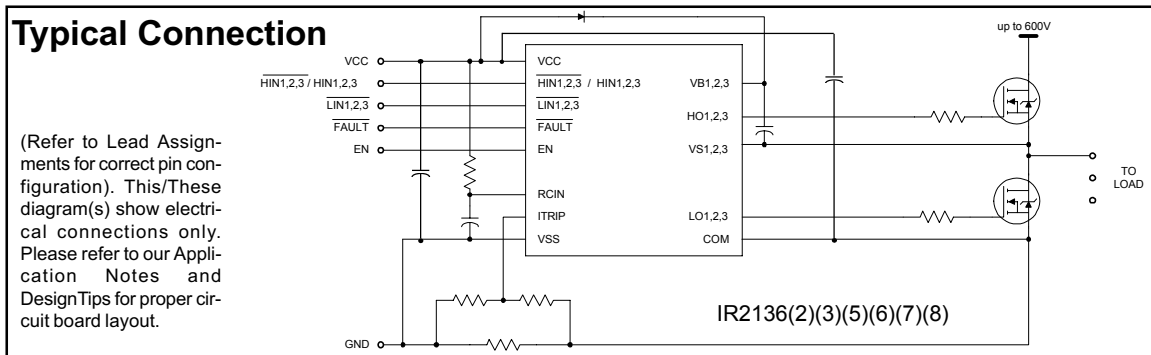


Feature Comparison: IR2136/IR21362/IR21363/ IR21365/IR21366/IR21367/IR21368

Part	IR2136	IR21362	IR21363	IR21365	IR21366	IR21367	IR21368
Input Logic	HIN, LIN	HIN/LIN	HIN, LIN	HIN, LIN	HIN, LIN	HIN, LIN	HIN, LIN
Ton (typ.)	400ns	400ns	400ns	400ns	250ns	250ns	400ns
Toff (typ.)	380ns	380ns	380ns	380ns	180ns	180ns	380ns
V _{IH} (typ.)	2.7V	2.7V	2.7V	2.7V	2.0V	2.0V	2.0V
V _{IL} (typ.)	1.7V	1.7V	1.7V	1.7V	1.3V	1.3V	1.3V
V _{itrip+}	0.46V	0.46V	0.46V	4.3V	0.46V	4.3V	4.3V
UV CC/BS+	8.9V	10.4V	11.2V	11.2V	11.2V	11.2V	8.9V
UV CC/BS-	8.2V	9.4V	11.0V	11.0V	11.0V	11.0V	8.2V

Description

The IR2136/IR21362/IR21363/IR21365/IR21366/IR21367/IR21368(J&S) are high voltage, high speed power MOSFET and IGBT drivers with three independent high and low side referenced output channels for 3-phase applications. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. An enable function is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that an overcurrent or undervoltage shutdown has occurred. Overcurrent fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 volts.



IR2136(2)(3)(5)(6)(7)(8)(J&S) & (PbF)

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V _S	High side offset voltage	V _{B1,2,3} - 25	V _{B1,2,3} + 0.3	V	
V _{BS}	High side floating supply voltage	-0.3	625		
V _{HO}	High side floating output voltage	V _{S1,2,3} - 0.3	V _{B1,2,3} + 0.3		
V _{CC}	Low side and logic fixed supply voltage	-0.3	25		
V _{SS}	Logic ground	V _{CC} - 25	V _{CC} + 0.3		
V _{LO1,2,3}	Low side output voltage	-0.3	V _{CC} + 0.3		
V _{IN}	Input voltage LIN,HIN,ITRIP, EN, RCIN	V _{SS} - 0.3	lower of (V _{SS} + 15) or V _{CC} + 0.3)		
V _{FLT}	FAULT output voltage	V _{SS} - 0.3	V _{CC} + 0.3		
dV/dt	Allowable offset voltage slew rate	—	50	V/ns	
P _D	Package power dissipation @ T _A ≤ +25°C	(28 lead PDIP)	—	1.5	W
		(28 lead SOIC)	—	1.6	
		(44leadPLCC)	—	2.0	
R _{thJA}	Thermal resistance, junction to ambient	(28 lead PDIP)	—	83	°C/W
		(28 lead SOIC)	—	78	
		(44 lead PLCC)	—	63	
T _J	Junction temperature	—	150	°C	
T _S	Storage temperature	-55	150		
T _L	Lead temperature (soldering, 10 seconds)	—	300		

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute referenced to COM. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units	
V _{B1,2,3}	High side floating supply voltage	IR2136(8)	V _{S1,2,3} +10	V _{S1,2,3} +20	V
		IR21362	V _{S1,2,3} +11.5	V _{S1,2,3} +20	
		IR2136(3)(5)(6)(7)	V _{S1,2,3} +12	V _{S1,2,3} +20	
V _{S1,2,3}	High side floating supply offset voltage	Note 1	600		
V _{HO1,2,3}	High side output voltage	V _{S1,2,3}	V _{B1,2,3}		
V _{LO1,2,3}	Low side output voltage	0	V _{CC}		
V _{CC}	Low side and logic fixed supply voltage	IR2136(8)	10	20	
		IR21362	11.5	20	
		IR2136(3)(5)(6)(7)	12	20	
V _{SS}	Logic ground	-5	5		
V _{FLT}	FAULT output voltage	V _{SS}	V _{CC}		
V _{RCIN}	RCIN input voltage	V _{SS}	V _{CC}		

Note 1: Logic operational for V_S of COM -5V to COM +600V. Logic state held for V_S of COM -5V to COM -V_{BS}.
(Please refer to the Design Tip DT97-3 for more details).

Note 2: All input pins and the ITRIP pin are internally clamped with a 5.2V zener diode.

Recommended Operating Conditions cont.

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute referenced to COM. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_{ITRIP}	ITRIP input voltage	V_{SS}	$V_{SS} + 5$	V
V_{IN}	Logic input voltage \overline{LIN} , \overline{HIN} (IR2136,IR21363(5)(6)(7)(8)), \overline{HIN} (IR21362), EN	V_{SS}	$V_{SS} + 5$	
T_A	Ambient temperature	-40	125	°C

Note 2: All input pins and the ITRIP pin are internally clamped with a 5.2V zener diode.

Static Electrical Characteristics

V_{BIAS} (V_{CC} , $V_{BS1,2,3}$) = 15V unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels ($H_{S1,2,3}$ and $L_{S1,2,3}$). The V_O and I_O parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: $H_{O1,2,3}$ and $L_{O1,2,3}$.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions	
V_{IH}	Logic "0" input voltage $\overline{LIN1,2,3}$, $\overline{HIN1,2,3}$ IR2136(3)(5)	3.0	—	—	V		
	Logic "1" input voltage $\overline{HIN1,2,3}$ IR21362						
	Logic "0" input voltage $\overline{LIN1,2,3}$, $\overline{HIN1,2,3}$ IR21366(7)(8)	2.5	—	—			
V_{IL}	Logic "1" input voltage $\overline{LIN1,2,3}$, $\overline{HIN1,2,3}$ IR2136(3)(5)	—	—	0.8			
	Logic "0" input voltage $\overline{HIN1,2,3}$ IR21362						
	Logic "0" input voltage $\overline{LIN1,2,3}$, $\overline{HIN1,2,3}$ IR21366(7)(8)	—	—	0.8			
$V_{EN,TH+}$	EN positive going threshold	—	—	3			
$V_{EN,TH-}$	EN negative going threshold	0.8	—	—			
$V_{IT,TH+}$	ITRIP positive going threshold	IR2136(2)(3)(6)	0.37	0.46		0.55	
		IR21365(7)(8)	3.85	4.30		4.75	
$V_{IT,HYS}$	ITRIP input hysteresis	IR2136(2)(3)(6)	—	0.07	—		
		IR21365(7)(8)	—	.15	—		
$V_{RCIN,TH+}$	RCIN positive going threshold	—	8	—			
$V_{RCIN,HYS}$	RCIN input hysteresis	—	3	—			
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	0.9	1.4		$I_O = 20\text{ mA}$	
V_{OL}	Low level output voltage, V_O	—	0.4	0.6		$I_O = 20\text{ mA}$	
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	IR2136(8)	8.0	8.9	9.8		
		IR21362	9.6	10.4	11.2		
		IR21363(5)(6)(7)	10.6	11.1	11.6		

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Static Electrical Characteristics cont.

V_{BIAS} (V_{CC} , $V_{BS1,2,3}$) = 15V unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels ($H_{S1,2,3}$ and $L_{S1,2,3}$). The V_O and I_O parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: $H_{O1,2,3}$ and $L_{O1,2,3}$.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions	
V_{CCUV} - V_{BSUV} -	V_{CC} and V_{BS} supply undervoltage negative going threshold	IR2136(8) IR21362 IR21363(5)(6)(7)	7.4 8.6 10.4	8.2 9.4 10.9	9.0 10.2 11.4	V	
V_{CCUVH} V_{BSUVH}	V_{CC} and V_{BS} supply undervoltage lockout hysteresis	IR2136 IR21362 IR21363(5)	0.3 0.5 —	0.7 1.0 0.2	— — —	V	
I_{LK}	Offset supply leakage current	—	—	50	μA	$V_{B1,2,3}=V_{S1,2,3}=600V$	
I_{QBS}	Quiescent V_{BS} supply current	—	70	120	μA		
I_{QCC}	Quiescent V_{CC} supply current	—	1.6	2.3	mA	$V_{IN} = 0V$ or $5V$	
$V_{IN, CLAMP}$	Input clamp voltage (H_{IN} , L_{IN} , I_{TRIP} and EN)	4.9	5.2	5.5	V	$I_{IN} = 100\mu A$	
I_{LIN+}	Input bias current ($L_{OUT} = HI$)	IR2136(2)(3)(5) IR21366(7)(8)	— —	200 0	300 1	μA	$V_{LIN} = 5V$
I_{LIN-}	Input bias current ($L_{OUT} = LO$)	IR2136(2)(3)(5) IR21366(7)(8)	— —	100 0	220 1	μA	$V_{LIN} = 0V$
I_{HIN+}	Input bias current ($H_{OUT} = HI$)	IR2136(3)(5) IR21362 IR21366(7)(8)	— — —	200 30 0	300 100 1	μA	$V_{HIN} = 5V$
I_{HIN-}	Input bias current ($H_{OUT} = LO$)	IR2136(3)(5) IR21362(6)(7)(8)	— —	100 0	220 1	μA	$V_{HIN} = 0V$
I_{ITRIP+}	"high" I_{TRIP} input bias current	—	30	100	μA	$V_{ITRIP} = 5V$	
I_{ITRIP-}	"low" I_{TRIP} input bias current	—	0	1	μA	$V_{ITRIP} = 0V$	
I_{EN+}	"high" EN input bias current	—	30	100	μA	$V_{ENABLE} = 5V$	
I_{EN-}	"low" EN input bias current	—	0	1	μA	$V_{ENABLE} = 0V$	
I_{RCIN}	$RCIN$ input bias current	—	0	1	μA	$V_{RCIN} = 0V$ or $15V$	
I_{O+}	Output high short circuit pulsed current	120	200	—	mA	$V_O = 0V$, $PW \leq 10 \mu s$	
I_{O-}	Output low short circuit pulsed current	250	350	—	mA	$V_O = 15V$, $PW \leq 10 \mu s$	
$R_{ON, RCIN}$	$RCIN$ low on resistance	—	50	100	Ω		
$R_{ON, FLT}$	FAULT low on resistance	—	50	100	Ω		

Dynamic Electrical Characteristics

V_{CC} = V_{BS} = V_{BIAS} = 15V, V_{S1,2,3} = V_{SS} = COM, TA = 25°C and C_L = 1000 pF unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions			
t _{on}	Turn-on propagation delay IR2136(2)(3)(5)(8) IR21366(7)	300	425	550	nS	V _{IN} = 0 & 5V			
		—	250	—					
t _{off}	Turn-off propagation delay IR2136(2)(3)(5)(8) IR21366(7)	250	400	550					
		—	180	—					
t _r	Turn-on rise time	—	125	190					
t _f	Turn-off fall time	—	50	75					
t _{EN}	ENABLE low to output shutdown propagation delay IR2136(2)(3)(5)(8) IR21366(7)	300	450	600			mS	V _{IN} , V _{EN} = 0V or 5V	
		100	250	400					
t _{ITRIP}	ITRIP to output shutdown propagation delay	500	750	1000					V _{ITRIP} = 5V
t _{bl}	ITRIP blanking time	100	150	—					V _{IN} = 0V or 5V V _{ITRIP} = 5V
t _{FLT}	ITRIP to FAULT propagation delay	400	600	800	V _{IN} = 0V or 5V V _{ITRIP} = 5V				
t _{FILIN}	Input filter time (HIN, LIN, EN) (IR2136(2)(3)(5)(8) only)	100	200	—	V _{IN} = 0 & 5V				
t _{FLTCLR}	FAULT clear time RCIN: R=2meg, C=1nF	1.3	1.65	2	V _{IN} = 0V or 5V V _{ITRIP} = 0V				
DT	Deadtime	220	290	360	V _{IN} = 0 & 5V				
MT	Matching delay ON and OFF	—	40	75	nS	External dead time >400nsec			
MDT	Matching delay, max (t _{on} ,t _{off}) - min (t _{on} ,t _{off}), (t _{on} ,t _{off} are applicable to all 3 channels)	—	25	70					
PM	Output pulse width matching, PWin -PWout (fig.2)	—	40	75					

NOTE: For high side PWM, HIN pulse width must be ≥ 1μsec

VCC	VBS	ITRIP	ENABLE	FAULT	LO1,2,3	HO1,2,3
<UVCC	X	X	X	0 (note 1)	0	0
15V	<UVBS	0V	5V	high imp	LIN1,2,3	0
15V	15V	0V	5V	high imp	LIN1,2,3	HIN1,2,3
15V	15V	>V _{ITRIP}	5V	0 (note 2)	0	0
15V	15V	0V	0V	high imp	0	0

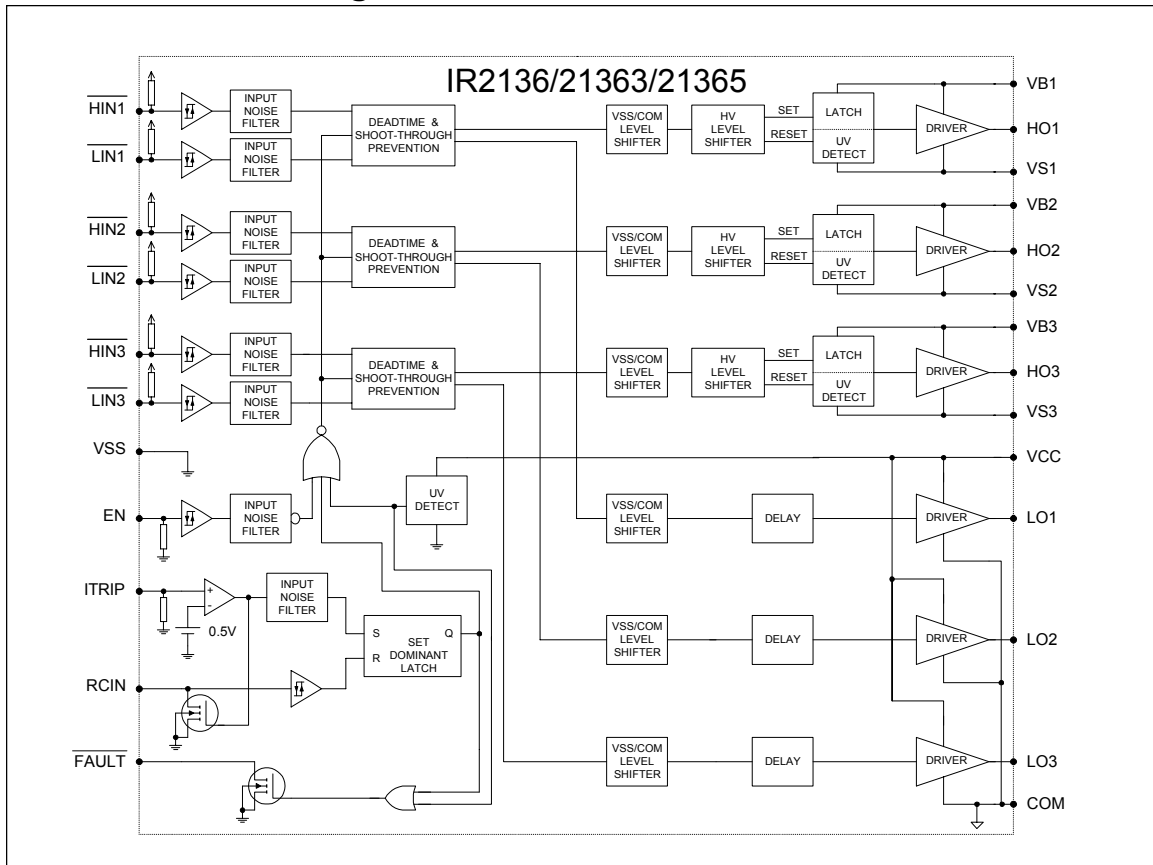
Note: A shoot-through prevention logic prevents LO1,2,3 and HO1,2,3 for each channel from turning on simultaneously.

Note 1: UVCC is not latched, when VCC>UVCC, FAULT returns to high impedance.

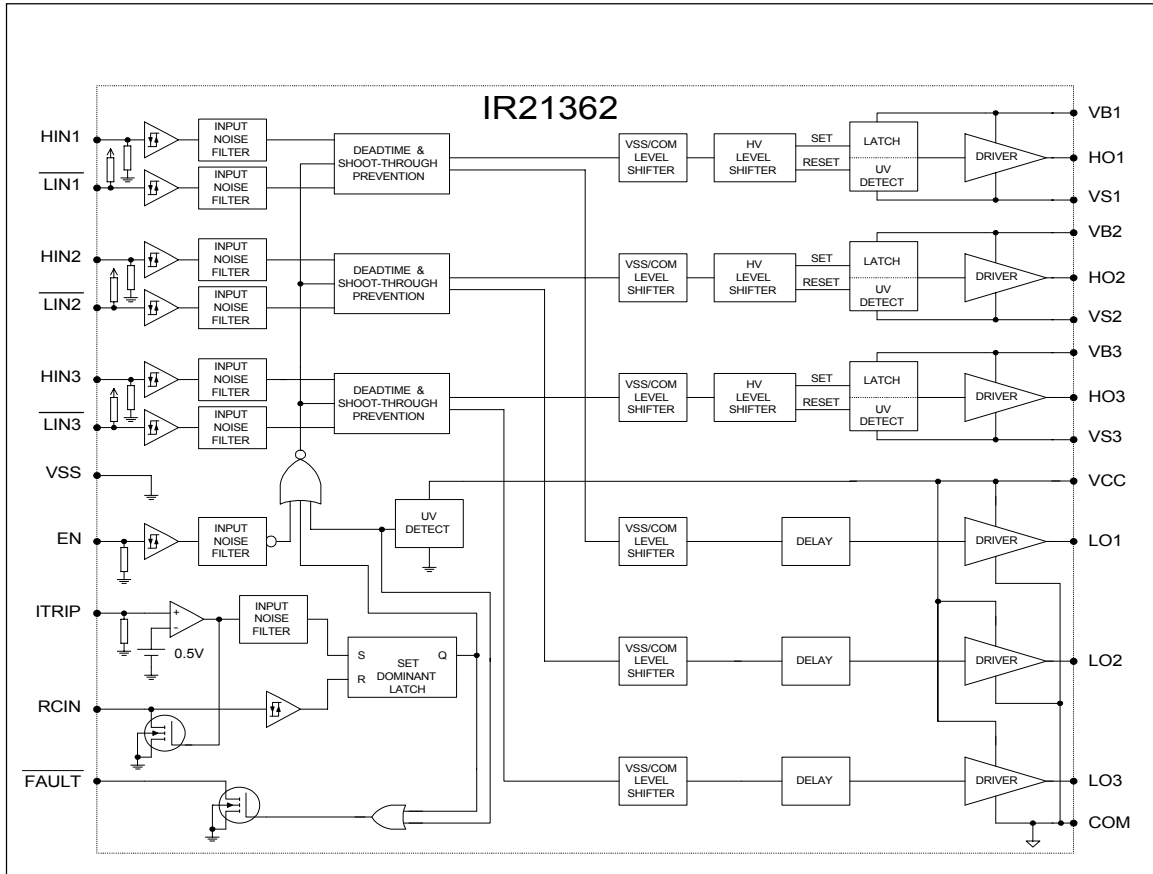
Note 2: When ITRIP <V_{ITRIP}, FAULT returns to high-impedance after RCIN pin becomes greater than 8V (@ VCC = 15V)

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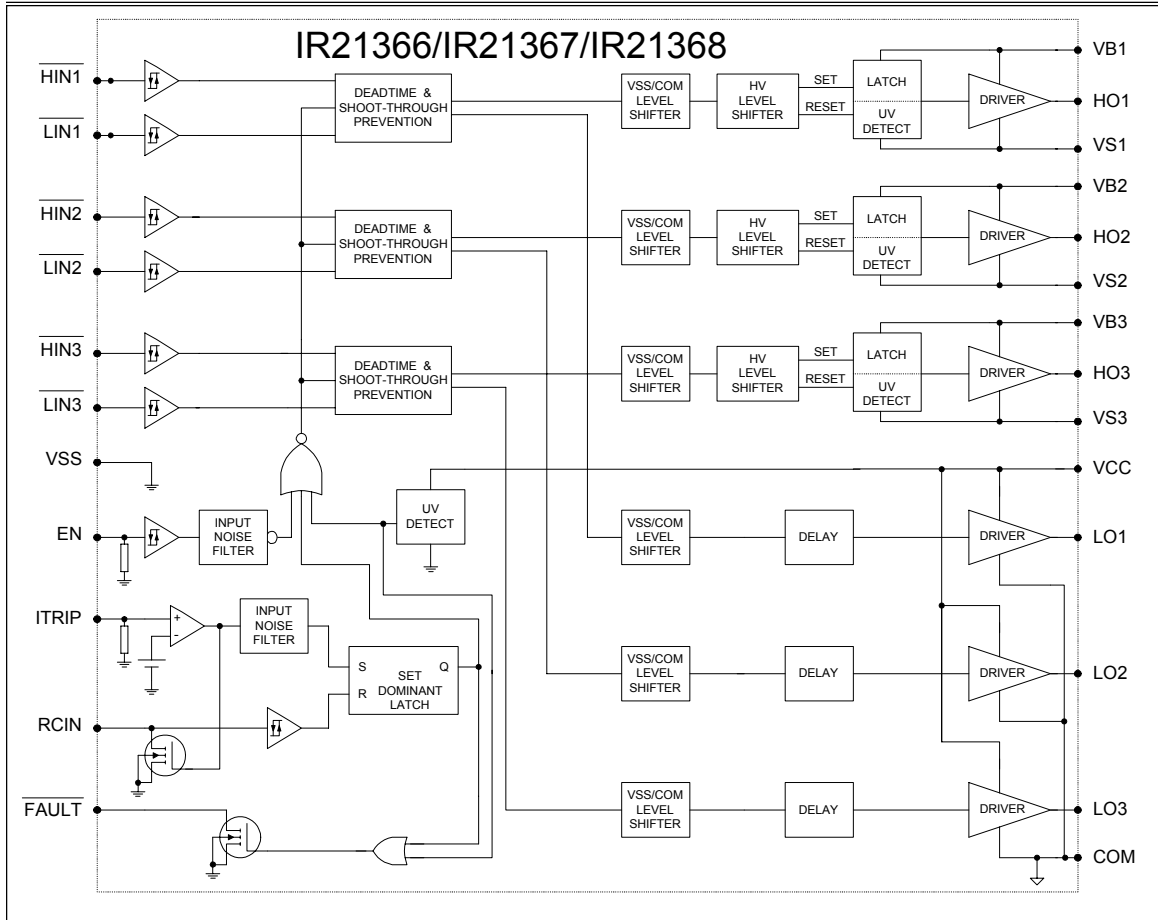
Functional Block Diagram



Functional Block Diagram



Functional Black Diagram



Lead Definitions

Symbol	Description
V _{CC}	Low side and logic fixed supply
V _{SS}	Logic Ground
HIN1,2,3	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase (IR2136/IR21363(5)(6)(7)(8))
HIN1,2,3	Logic inputs for high side gate driver outputs (HO1,2,3), in phase (IR21362)
LIN1,2,3	Logic inputs for low side gate driver outputs (LO1,2,3), out of phase
FAULT	Indicates over-current (ITRIP) or low-side undervoltage lockout has occurred. Negative logic, open-drain output
EN	Logic input to enable I/O functionality. Positive logic, i.e. I/O logic functions when ENABLE is high. No effect on FAULT and not latched
ITRIP	Analog input for overcurrent shutdown. When active, ITRIP shuts down outputs and activates FAULT and RCIN low. When ITRIP becomes inactive, FAULT stays active low for an externally set time T _{FLTCLR} , then automatically becomes inactive (open-drain high impedance).
RCIN	External RC network input used to define FAULT CLEAR delay, T _{FLTCLR} , approximately equal to R*C. When RCIN>8V, the FAULT pin goes back into open-drain high-impedance
COM	Low side gate driver return
V _B 1,2,3	High side floating supply
HO1,2,3	High side gate driver outputs
V _S 1,2,3	High voltage floating supply returns
LO1,2,3	Low side gate driver output

Note: All input pins and the ITRIP pin are internally clamped with a 5.2V zener diode.

IR2136(2)(3)(5)(6)(7)(8)(J&S) & (PbF)

Lead Assignments

<p>28 Lead PDIP</p>	<p>44 Lead PLCC w/o 12 leads</p>	<p>28 lead SOIC (wide body)</p>
<p>IR2136/IR21363(5)(6)(7)(8)</p>	<p>IR2136/IR21363(5)(6)(7)(8) (J)</p>	<p>IR2136/IR21363(5)(6)(7)(8) (S)</p>

<p>28 Lead PDIP</p>	<p>44 Lead PLCC w/o 12 leads</p>	<p>28 lead SOIC (wide body)</p>
<p>IR21362</p>	<p>IR21362J</p>	<p>IR21362S</p>

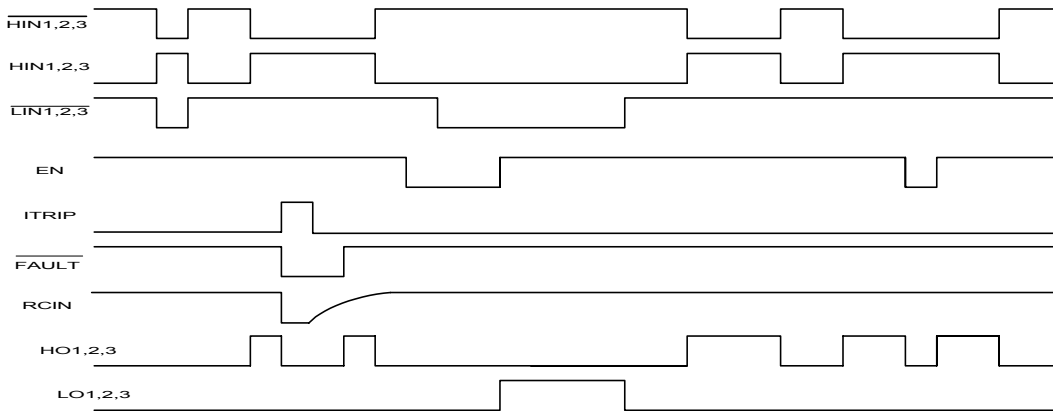


Figure 1. Input/Output Timing Diagram

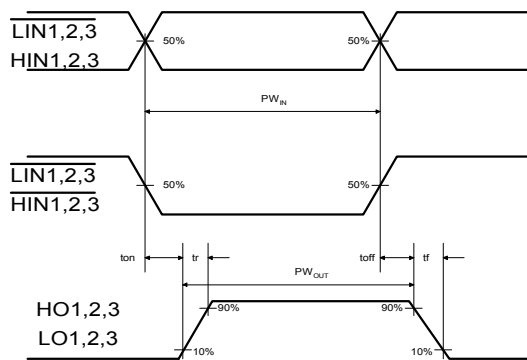


Figure 2. Switching Time Waveforms

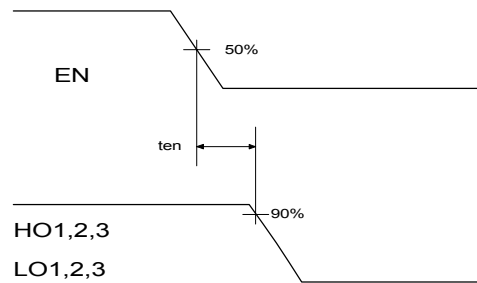


Figure 3. Output Enable Timing Waveform

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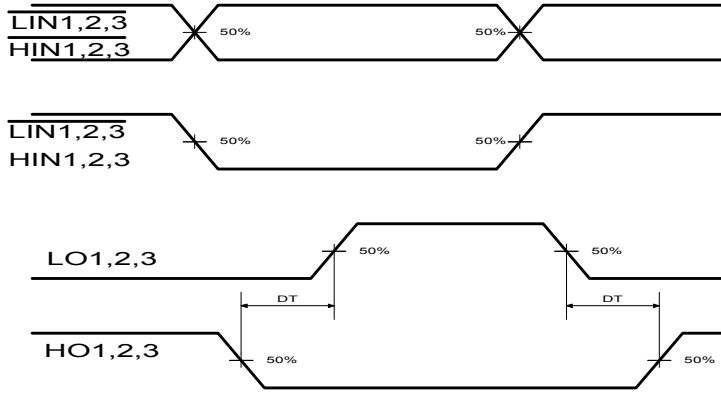


Figure 4. Internal Deadtime Timing Waveforms

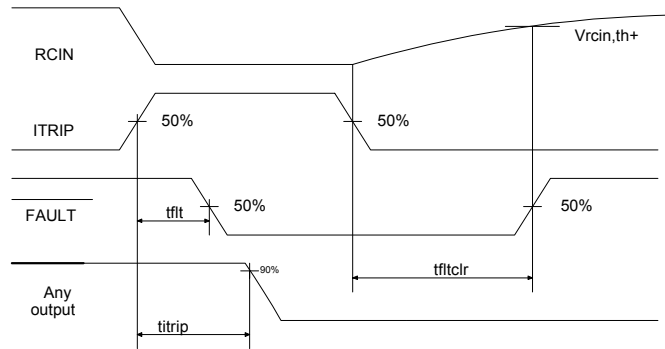


Figure 5. ITRIP/RCIN Timing Waveforms

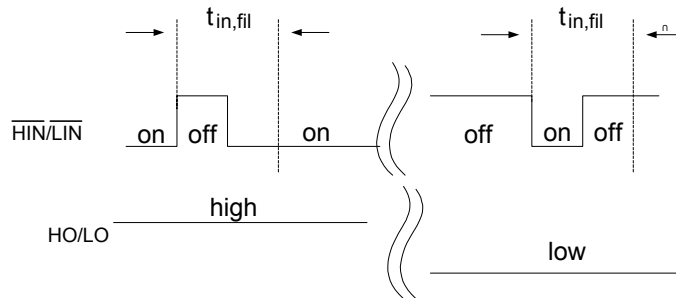


Figure 5.5 Input Filter Function

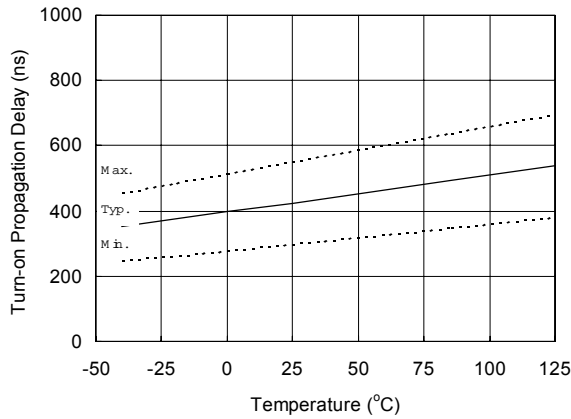


Figure 6A. Turn-on Propagation Delay vs. Temperature

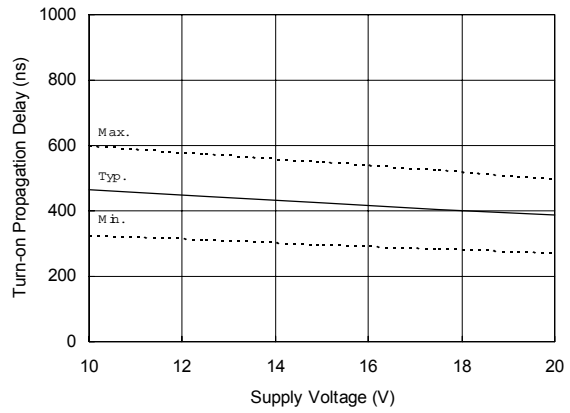


Figure 6B. Turn-on Propagation Delay vs. Supply Voltage

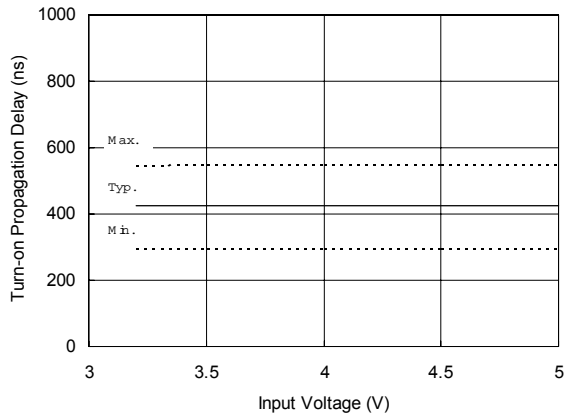


Figure 6C. Turn-on Propagation Delay vs. Input Voltage

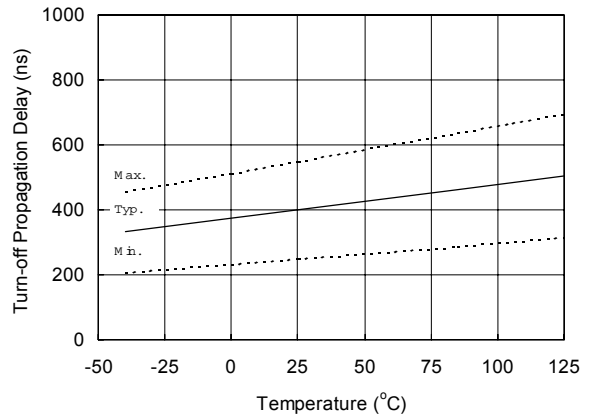


Figure 7A. Turn-off Propagation Delay vs. Temperature

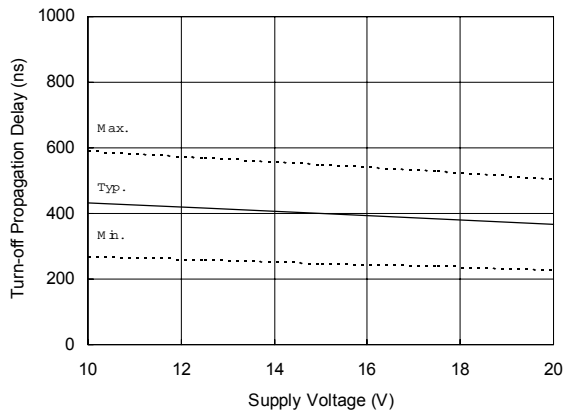


Figure 7B. Turn-off Propagation Delay vs. Supply Voltage

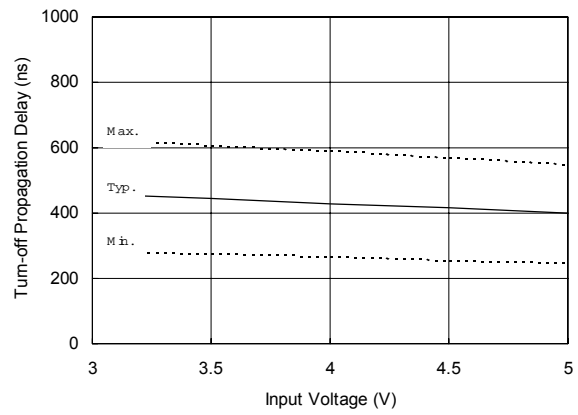


Figure 7C. Turn-off Propagation Delay vs. Input Voltage

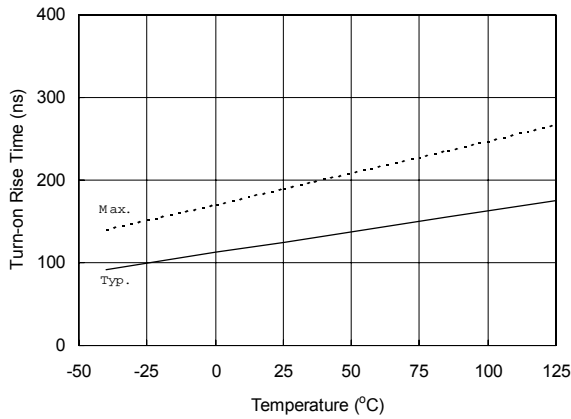


Figure 8A. Turn-on Rise Time vs. Temperature

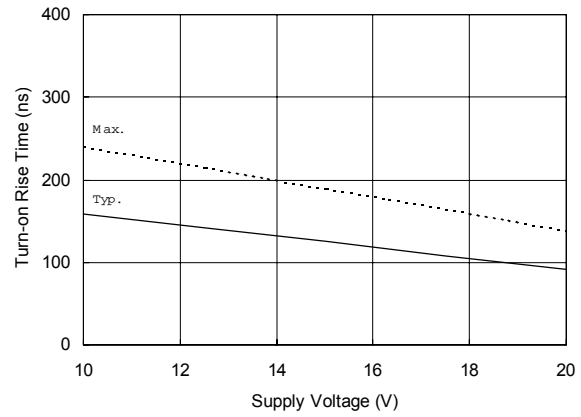


Figure 8B. Turn-on Rise Time vs. Supply Voltage

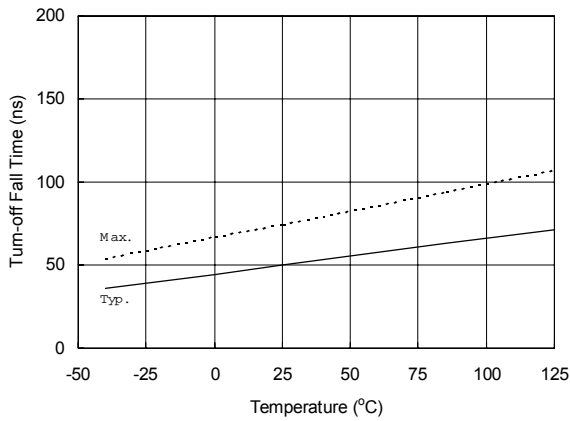


Figure 9A. Turn-off Fall Time vs. Temperature

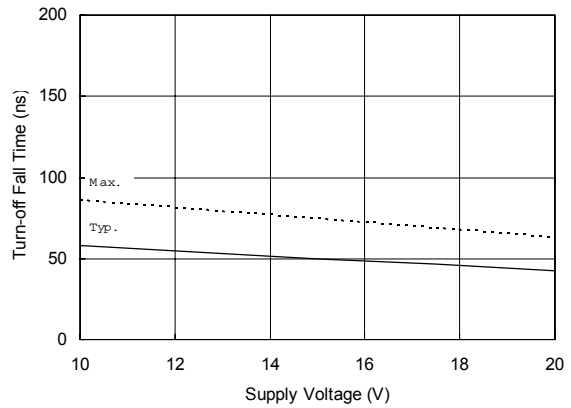


Figure 9B. Turn-off Fall Time vs. Supply Voltage

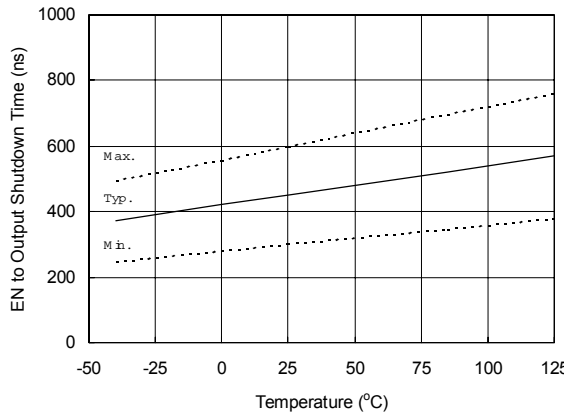


Figure 10A. EN to Output Shutdown Time vs. Temperature

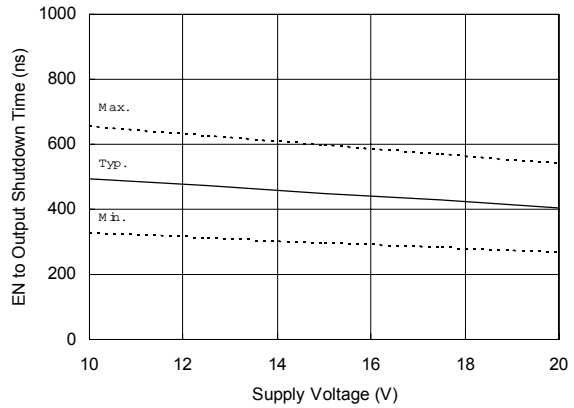


Figure 10B. EN to Output Shutdown Time vs. Supply Voltage

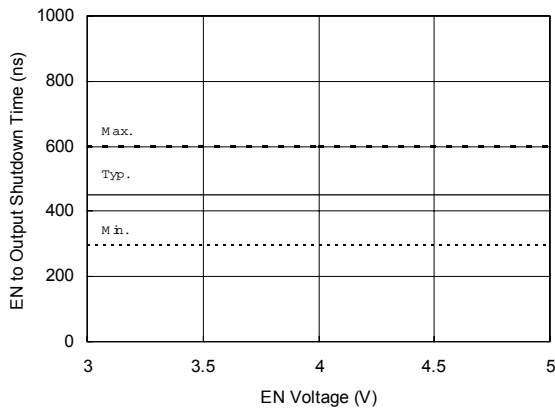


Figure 10C. EN to Output Shutdown Time vs. EN Voltage

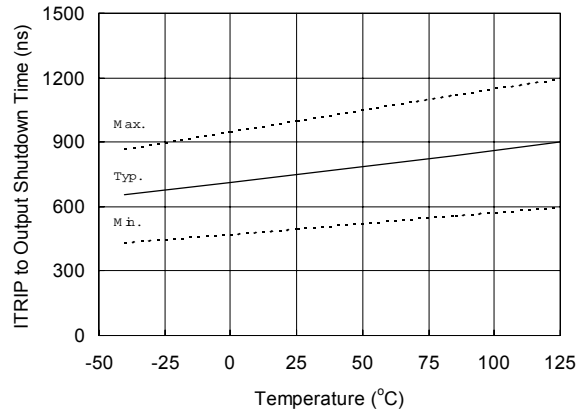


Figure 11A. ITRIP to Output Shutdown Time vs. Temperature

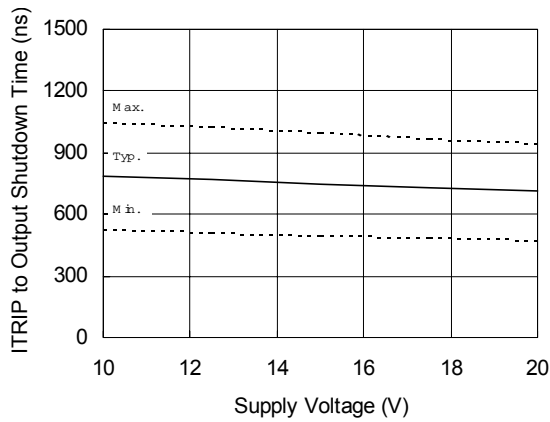


Figure 11B. ITRIP to Output Shutdown Time vs. Supply Voltage

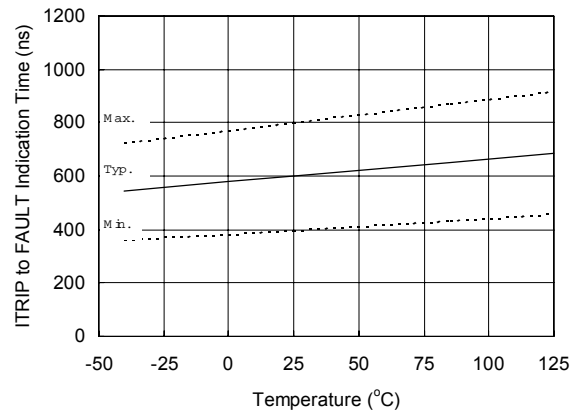


Figure 12A. ITRIP to FAULT Indication Time vs. Temperature

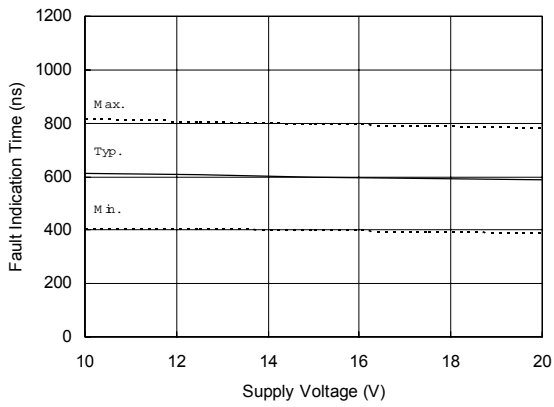


Figure 12B. ITRIP to FAULT Indication Time vs. Supply Voltage

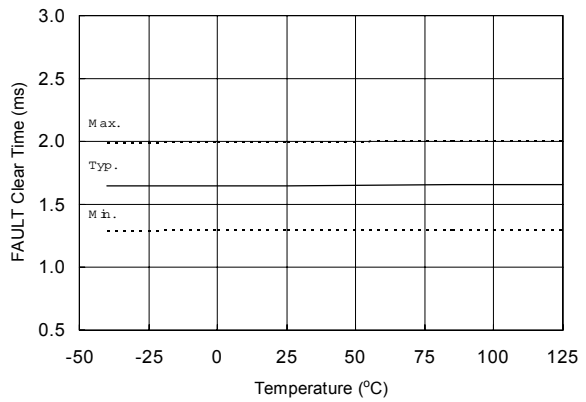


Fig13A. FAULT Clear Time vs. Temperature

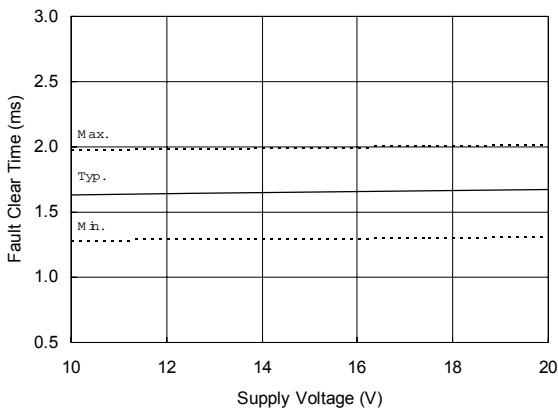


Figure 13B. FAULT Clear Time vs. Supply Voltage

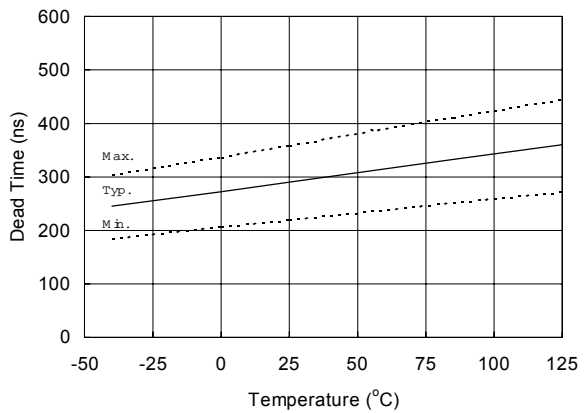


Figure 14A. Dead Time vs. Temperature

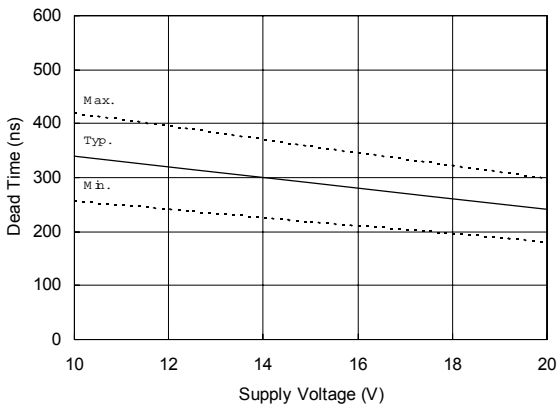


Figure 14B. Dead Time Time vs. Supply Voltage

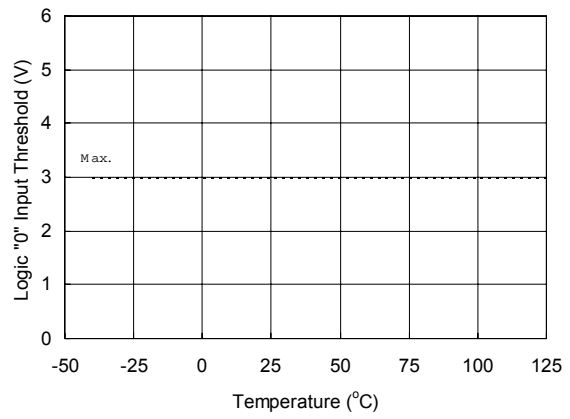


Figure 15A. Logic "0" Input Threshold vs. Temperature

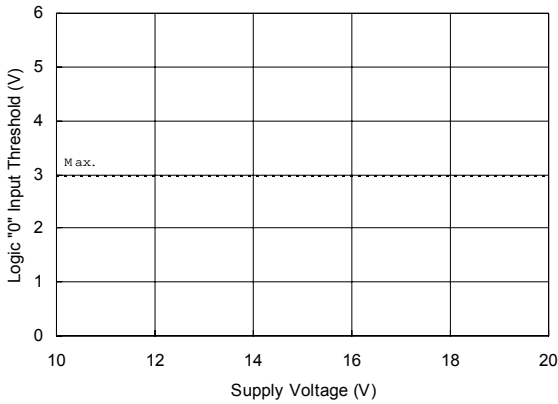


Figure 15B. Logic "0" Input Threshold vs. Supply Voltage

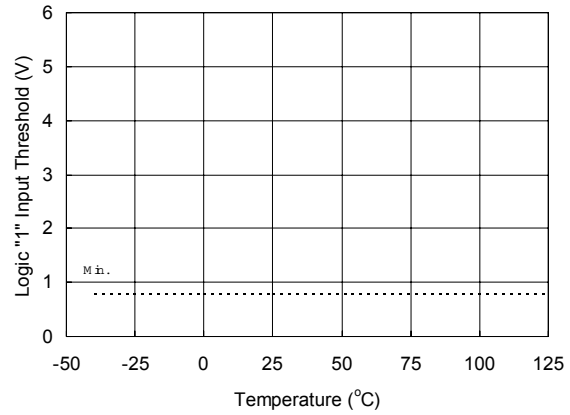


Figure 16A. Logic "1" Input Threshold vs. Temperature

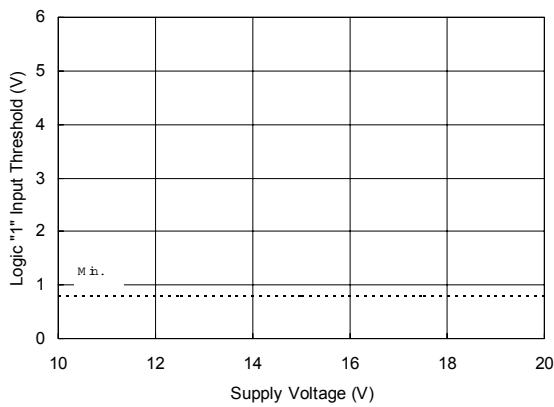


Figure 16B. Logic "1" Input Threshold vs. Supply Voltage

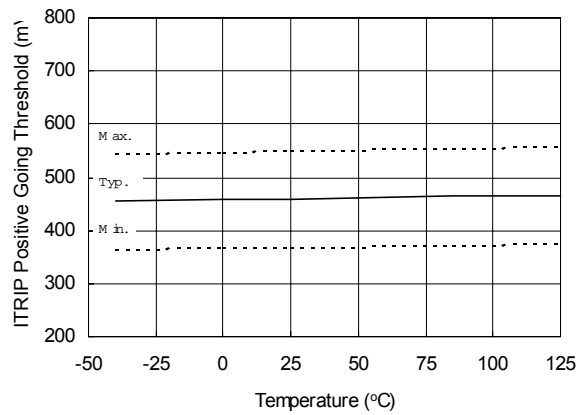


Figure 17A. ITRIP Positive Going Threshold vs. Temperature (IR2136/21362/21363/IR21366 Only)

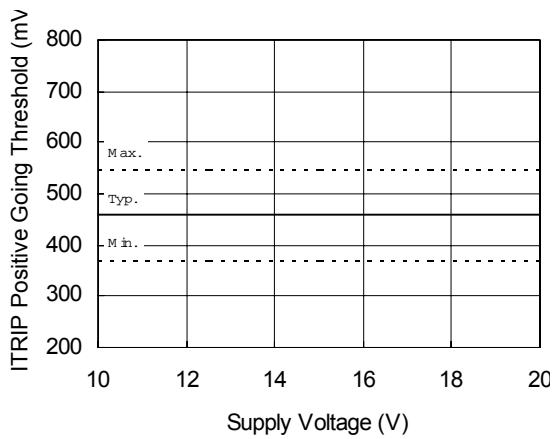


Figure 17B. ITRIP Positive Going Threshold vs. Supply Voltage (IR2136/21362/21363/IR21366 Only)

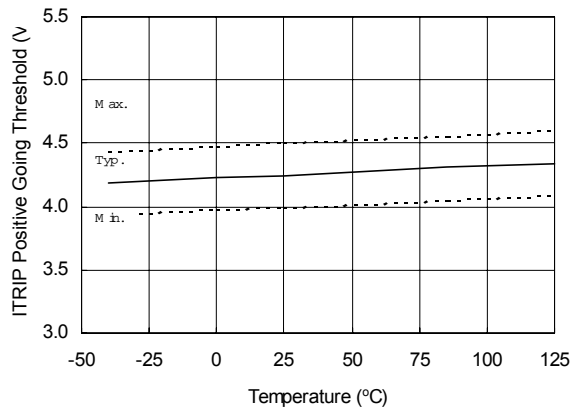


Figure 17C. ITRIP Positive Going Threshold vs. Temperature (IR21365/IR21367/IR21368 Only)

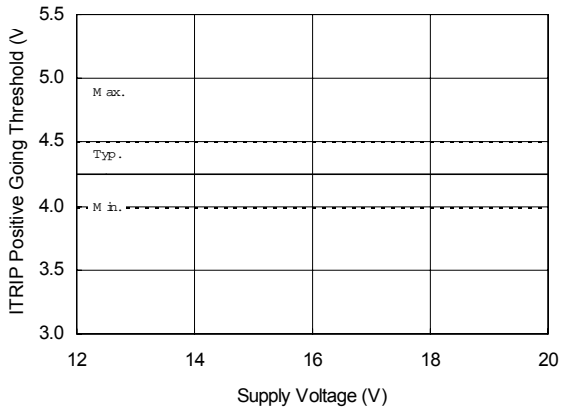


Figure 17D. ITRIP Positive Going Threshold vs. Supply Voltage (IR21365/IR21367/IR21368 Only)

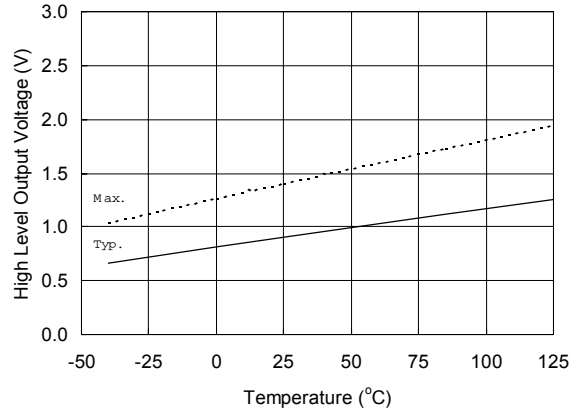


Figure 18A. High Level Output vs. Temperature

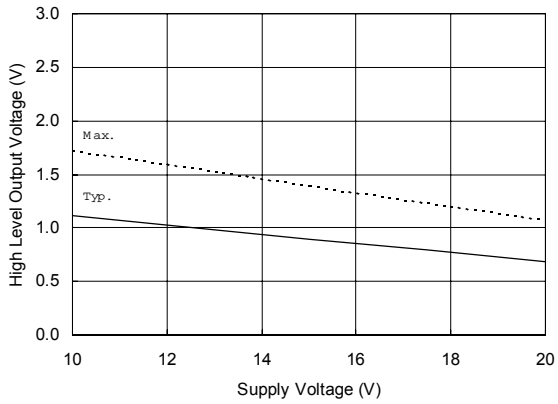


Figure 18B. High Level Output vs. Supply Voltage

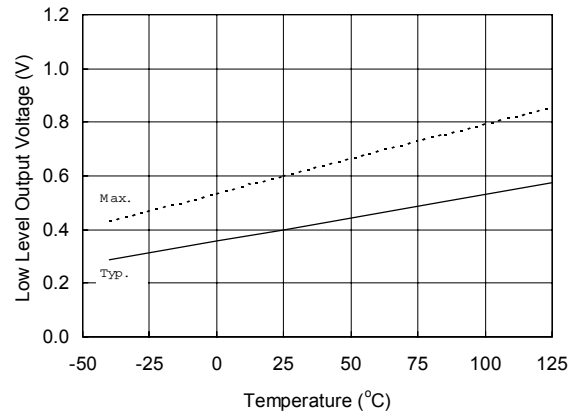


Figure 19A. Low Level Output vs. Temperature

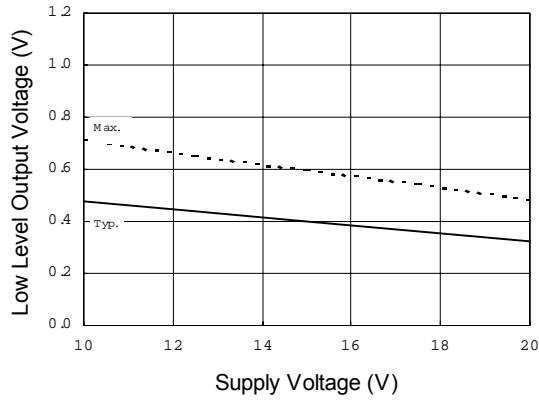


Figure 19B. Low Level Output vs. Supply Voltage

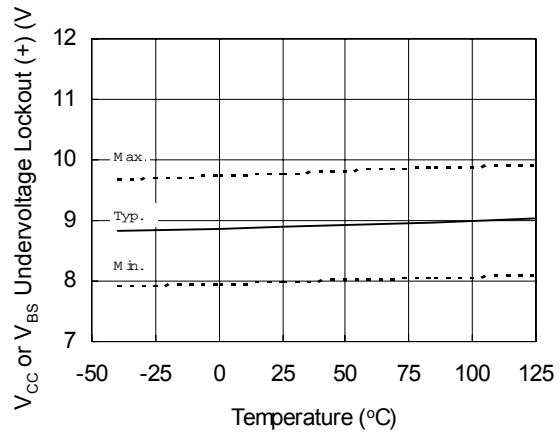


Figure 20. V_{CC} or V_{BS} Undervoltage (+) vs. Temperature (IR2136/IR21368 Only)

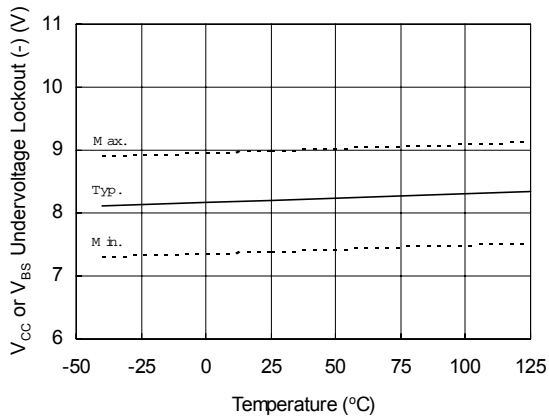


Figure 21. V_{CC} or V_{BS} Undervoltage (-) vs. Temperature (IR2136/IR21368 Only)

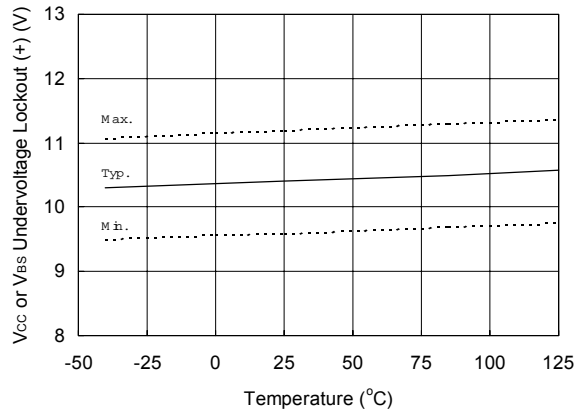


Figure 22. V_{CC} or V_{BS} Undervoltage (+) vs. Temperature (IR21362 Only)

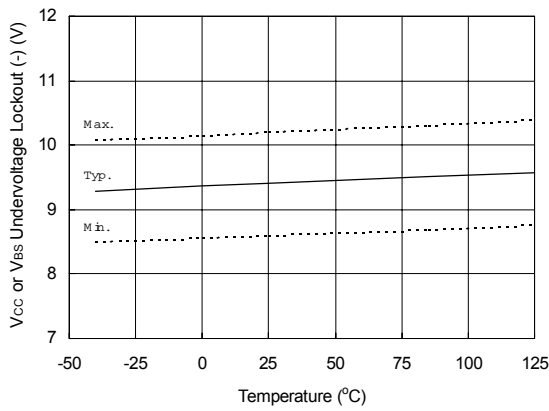


Figure 23. V_{CC} or V_{BS} Undervoltage Lockout (-) vs. Temperature (IR21362 Only)

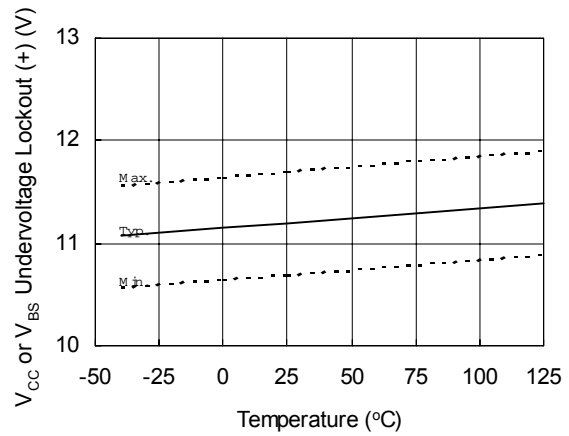


Figure 24. V_{CC} or V_{BS} Undervoltage Lockout (+) vs. Temperature (IR21363/21365/IR21366/IR21367 Only)

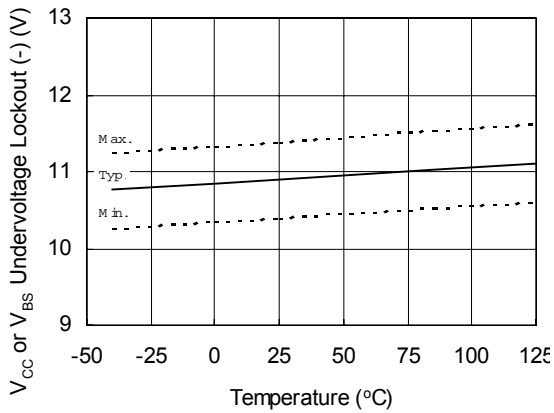


Figure 25. V_{CC} or V_{BS} Undervoltage Lockout (-) vs. Temperature (IR21363/21365/IR21366/IR21367 Only)

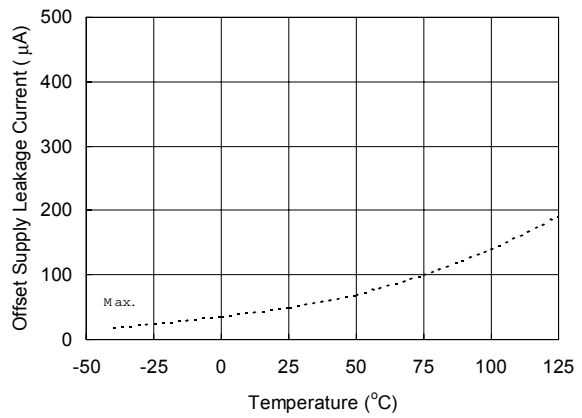


Figure 26A. Offset Supply Leakage Current vs. Temperature

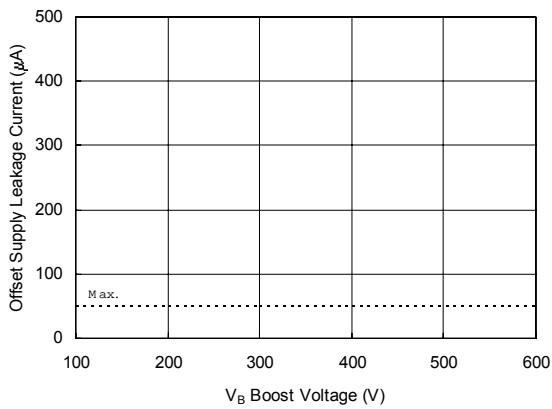


Figure 26B. Offset Supply Leakage Current vs. V_B Boost Voltage

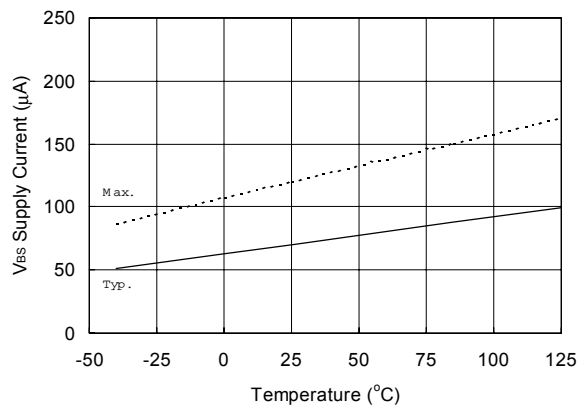


Figure 27A. V_{BS} Supply Current vs. Temperature

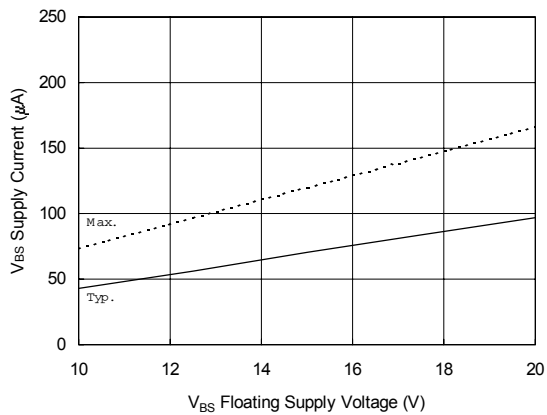


Figure 27B. V_{BS} Supply Current vs. V_{BS} Floating Supply Voltage

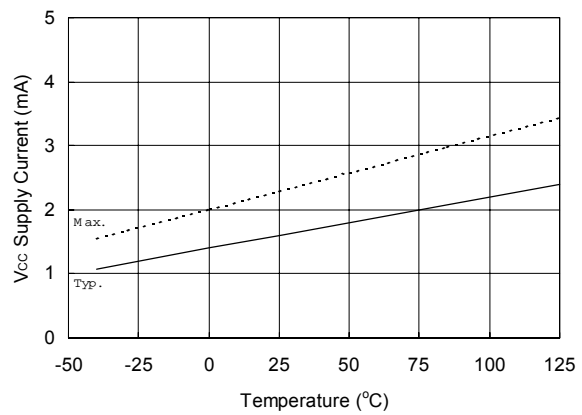


Figure 28A. V_{CC} Supply Current vs. Temperature

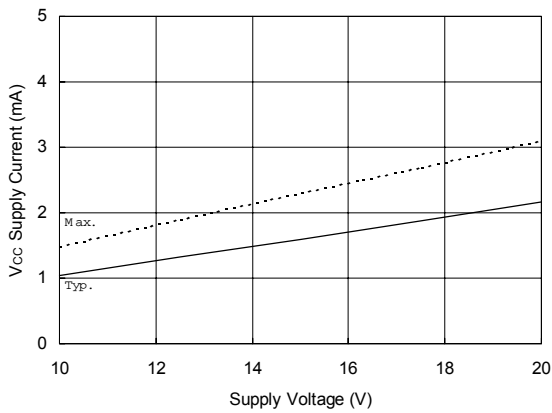


Figure 28B. V_{CC} Supply Current vs. V_{CC} Supply Voltage

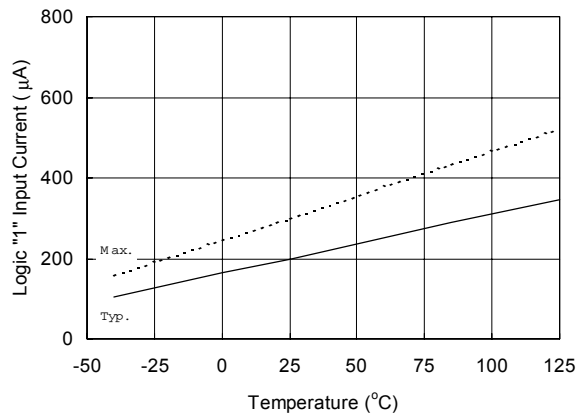


Figure 29A. Logic "1" Input Current vs. Temperature (IR2136/21363/21365 and IR21362 Low Side Only)

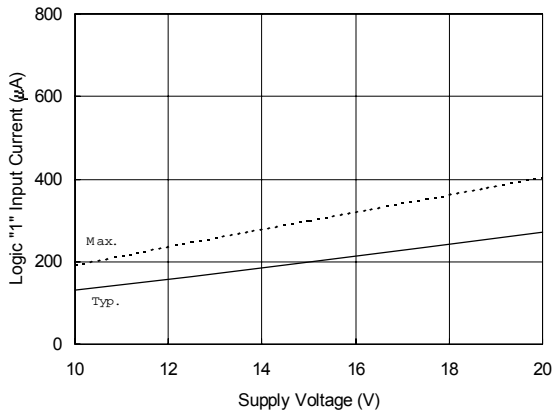


Figure 29B. Logic "1" Input Current vs. Supply Voltage (IR2136/21363/21365 and IR21362 Low Side Only)

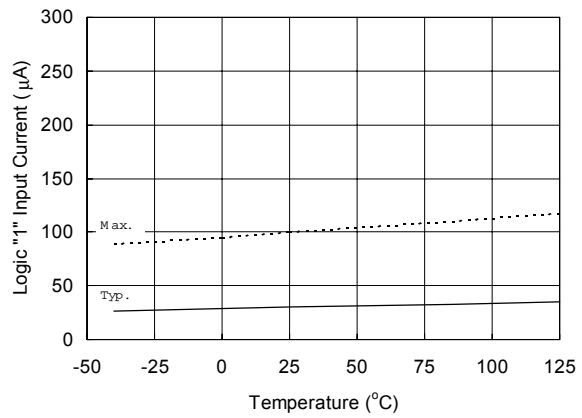


Figure 29C. Logic "1" Input Current vs. Temperature (IR21362 High Side Only)

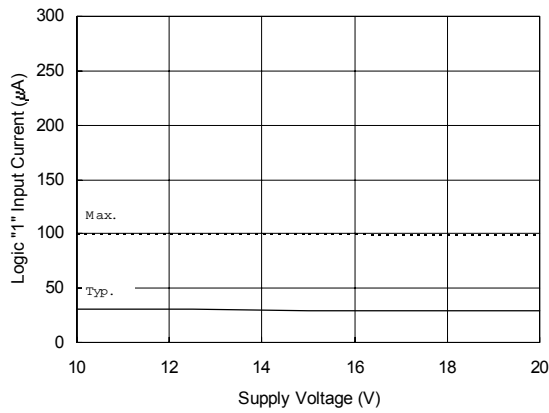


Figure 29D. Logic "1" Input Current vs. Supply Voltage (IR21362 High Side Only)

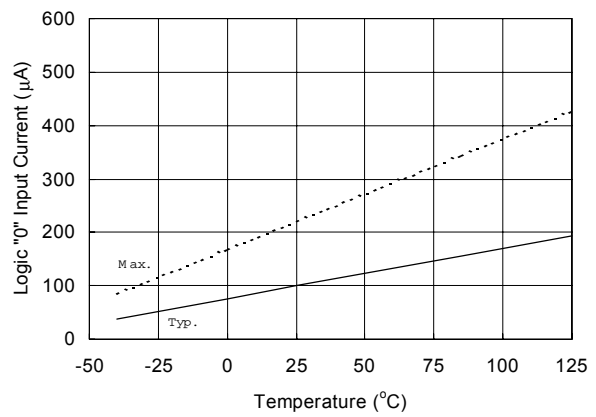


Figure 30A. Logic "0" Input Current vs. Temperature (IR2136/21363/21365 and IR21362 Low Side Only)

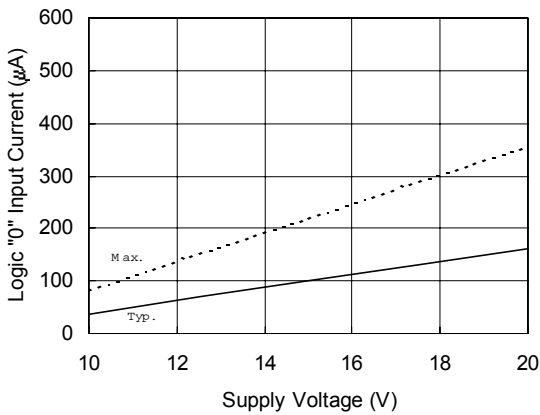


Figure 30B. Logic "0" Input Current vs. Supply Voltage (IR2136/21363/21365 and IR21362 Low Side Only)

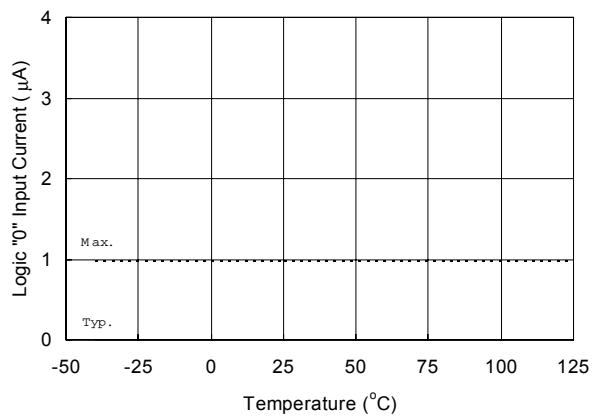


Figure 30C. Logic "0" Input Current vs. Temperature (IR21362 High Side Only)

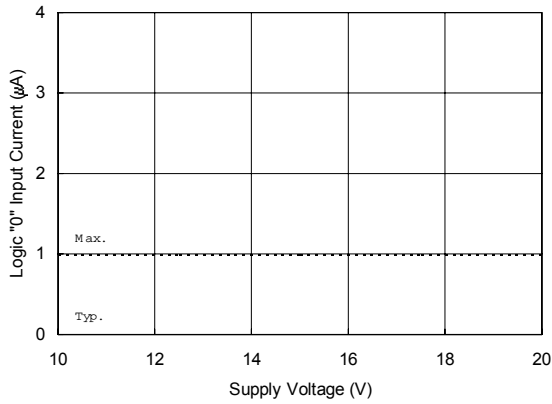


Figure 30D. Logic "0" Input Current vs. Supply Voltage (IR21362 High Side Only)

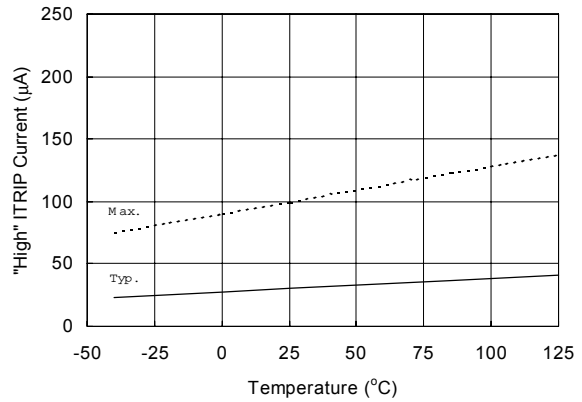


Figure 31A. "High" ITRIP Current vs. Temperature

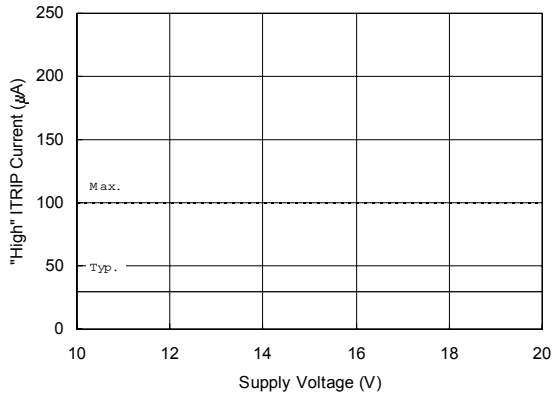


Figure 31B. "High" ITRIP Current vs. Supply Voltage

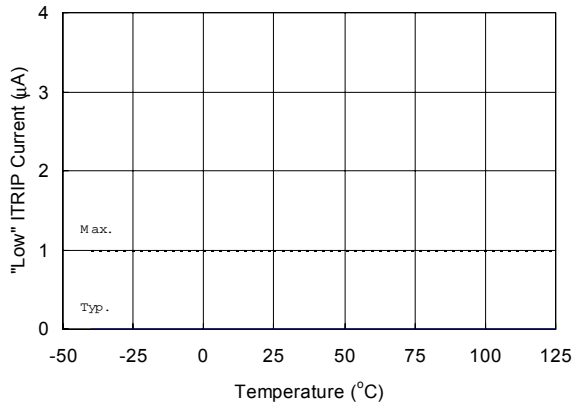


Figure 32A. "Low" ITRIP Current vs. Temperature

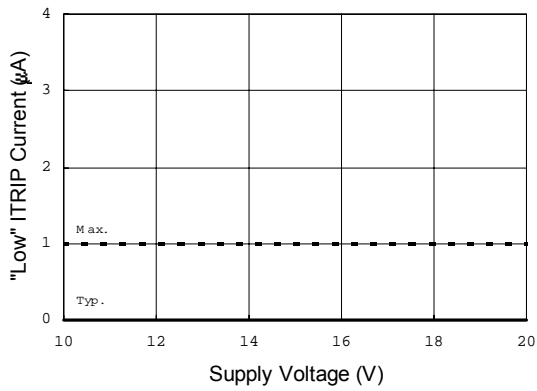


Figure 32B. "Low" ITRIP Current vs. Supply Voltage

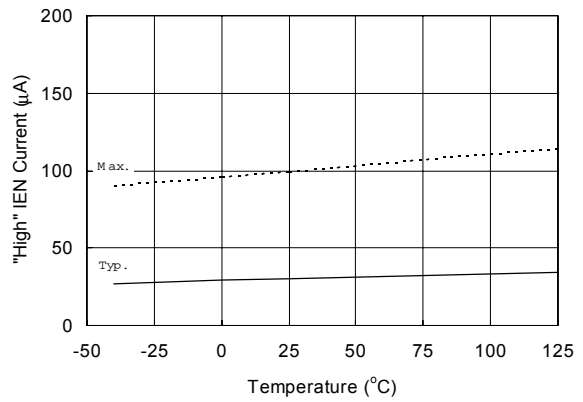


Figure 33A. "High" IEN Current vs. Temperature

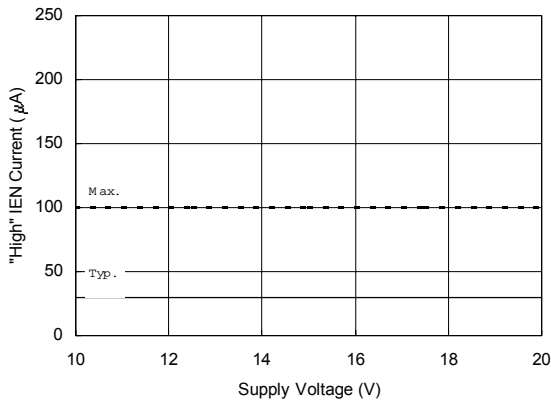


Figure 33B. "High" IEN Current vs. Supply Voltage

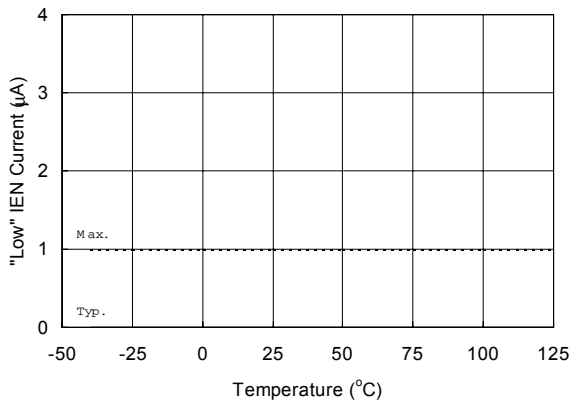


Figure 34A. "Low" IEN Current vs. Temperature

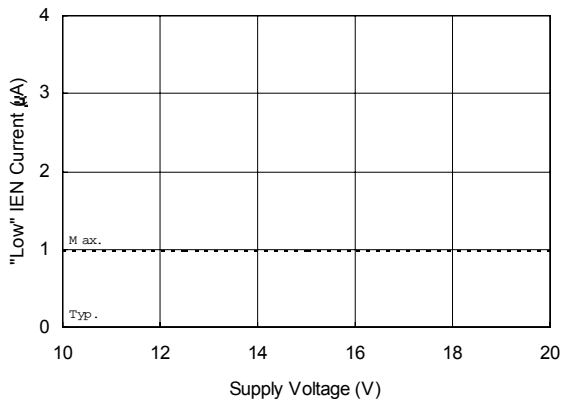


Figure 34B. "Low" IEN Current vs. Supply Voltage

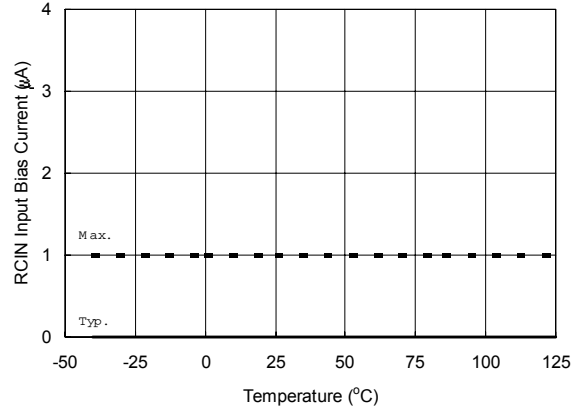


Figure 35A. RCIN Input Bias Current vs. Temperature

Figure 34B. "Low" IEN Current vs. Supply Voltage

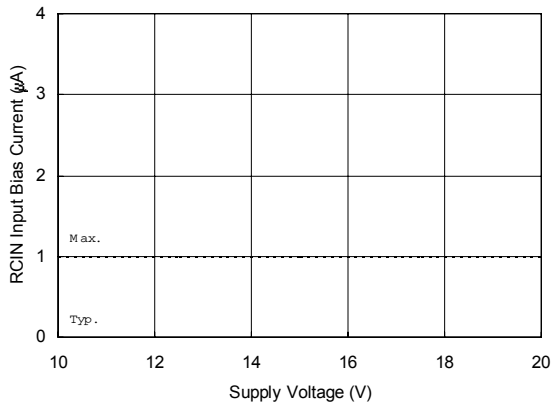


Figure 35B. RCIN Input Bias Current vs. Supply Voltage

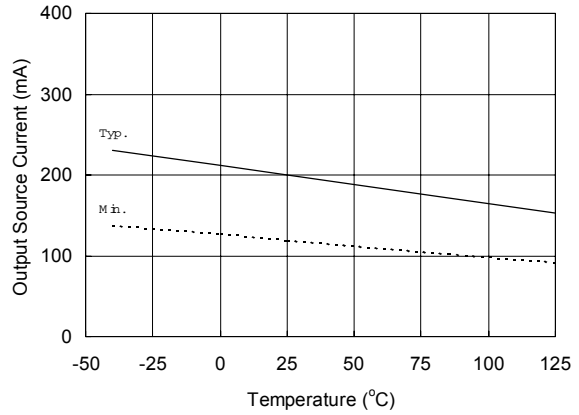


Figure 36A. Output Source Current vs. Temperature

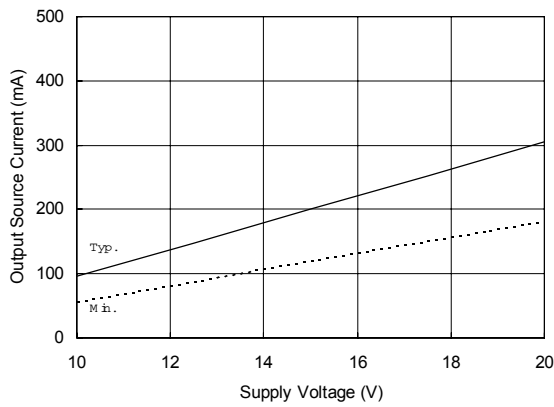


Figure 36B. Output Source Current vs. Supply Voltage

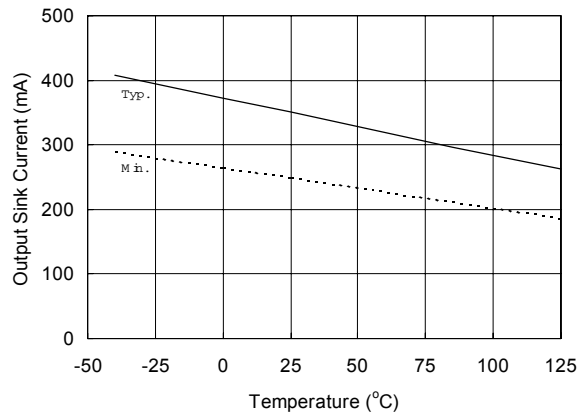


Figure 37A. Output Sink Current vs. Temperature

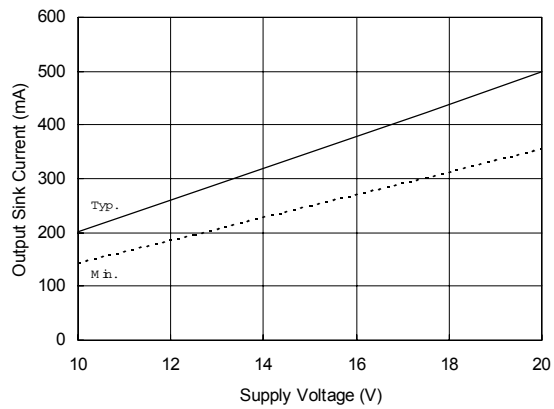


Figure 37B. Output Sink Current vs. Supply Voltage

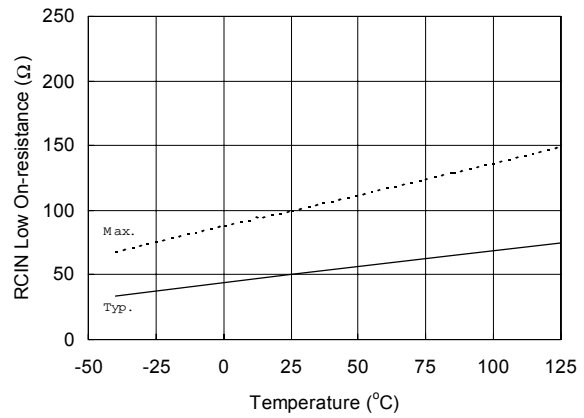


Figure 38A. RCIN Low On-resistance vs. Temperature

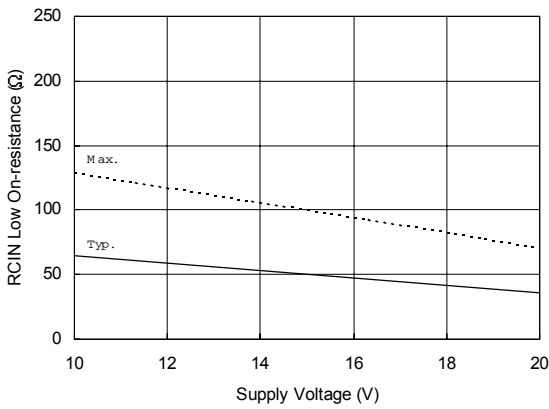


Figure 38B. RCIN Low On-resistance vs. Supply Voltage

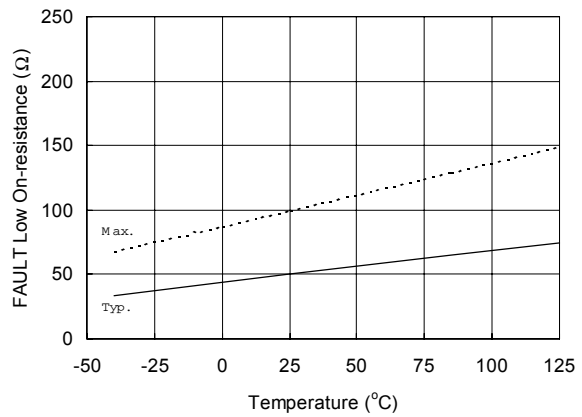


Figure 39A. FAULT Low On-resistance vs. Temperature

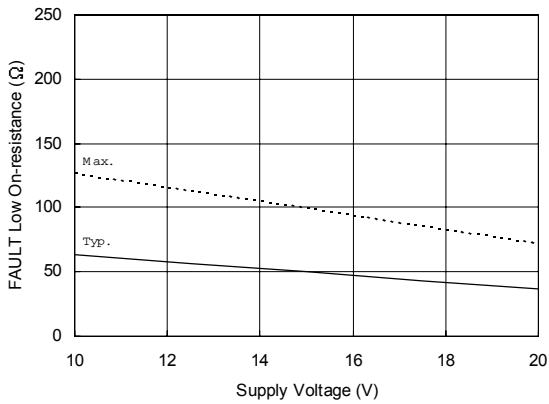


Figure 39B. FAULT Low On-resistance vs. Supply Voltage

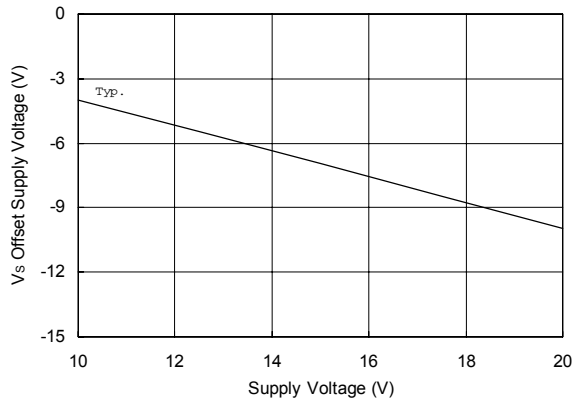
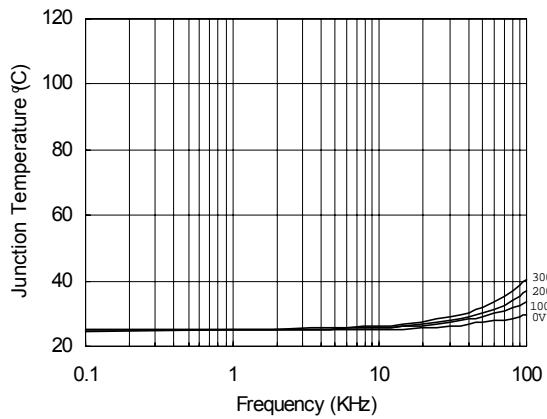
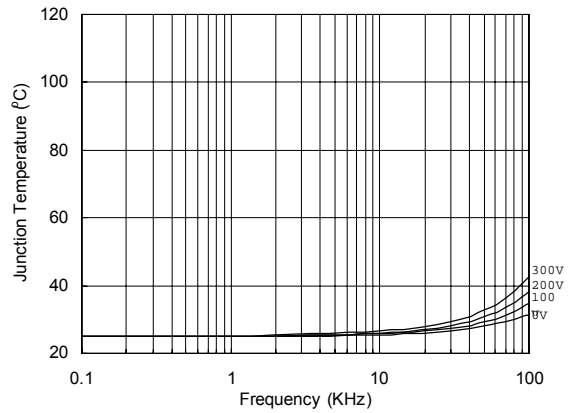


Figure 40. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

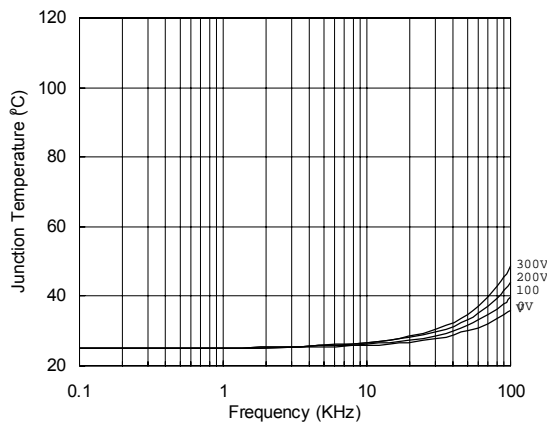
IR2136(2)(3)(5)(6)(7)(8)(J&S) & (PbF)



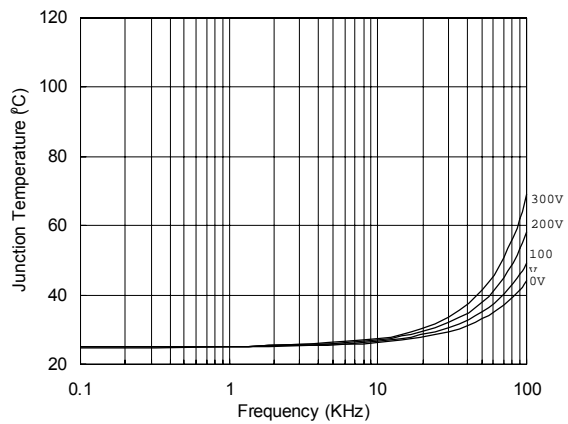
**Figure 41. IR2136/IR21362(3)(5)(6)(7)(8)
vs. Frequency (IRG4BC20W), R_{gate}=33Ω, V_{cc}=15V**



**Figure 42. IR2136/IR21362(3)(5)(6)(7)(8)
vs. Frequency (IRG4BC30W), R_{gate}=15Ω, V_{cc}=15V**



**Figure 43. IR2136/IR21362(3)(5)(6)(7)(8)
vs. Frequency (IRG4BC40W), R_{gate}=10Ω, V_{cc}=15V**



**Figure 44. IR2136/IR21362(3)(5)(6)(7)(8)
vs. Frequency (IRG4PC50W), R_{gate}=5Ω, V_{cc}=15V**

IR2136(2)(3)(5)(6)(7)(8)(J&S) & (PbF)

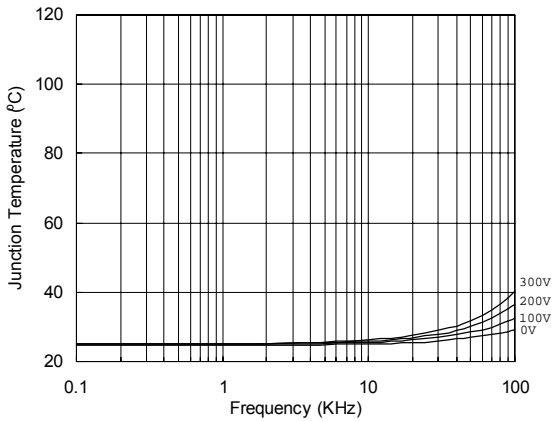


Figure 45. IR2136/IR21362(3)(5)(6)(7)(8) (J) vs. Frequency (IRG4BC20W), Rgate=33Ω, Vcc=15V

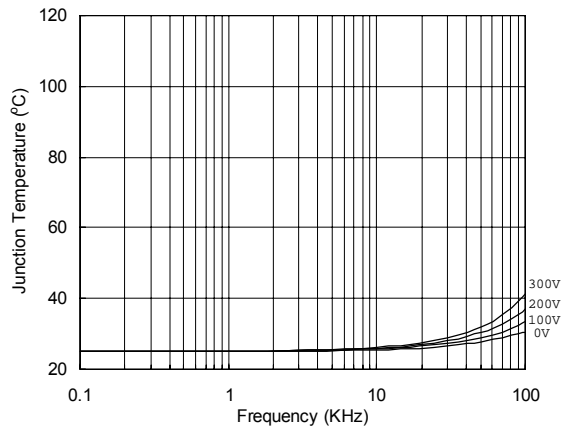


Figure 46. IR2136/IR21362(3)(5)(6)(7)(8) (J) vs. Frequency (IRG4BC30W), Rgate=15Ω, Vcc=15V

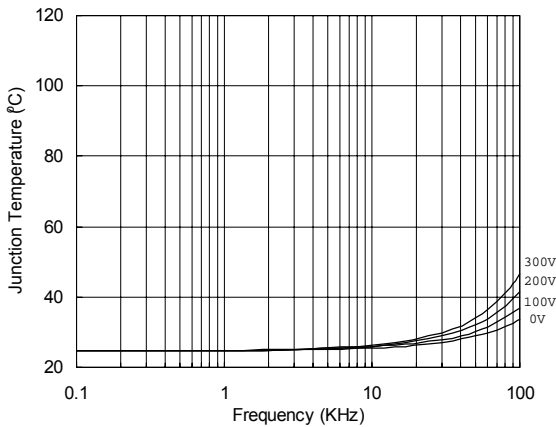


Figure 47. IR2136/IR21362(3)(5)(6)(7)(8) (J) vs. Frequency (IRG4BC40W), Rgate=10Ω, Vcc=15V

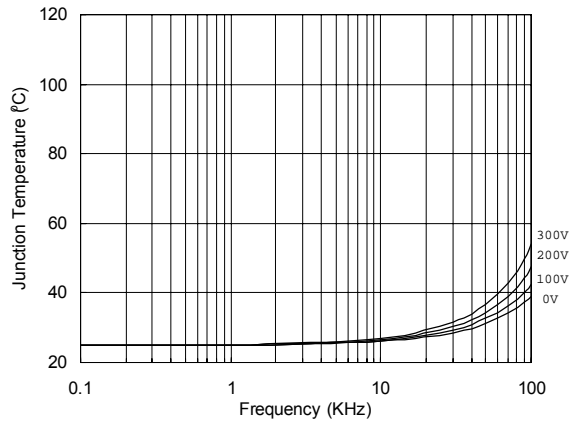


Figure 48. IR2136/IR21362(3)(5)(6)(7)(8) (J) vs. Frequency (IRG4PC50W), Rgate=5Ω, Vcc=15V

IR2136(2)(3)(5)(6)(7)(8)(J&S) & (PbF)

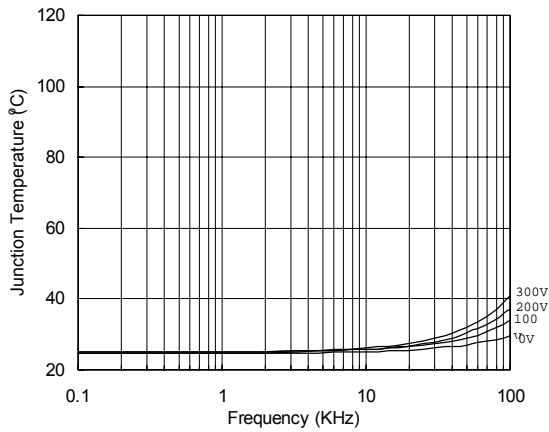


Figure 49. IR2136/IR21362(3)(5)(6)(7)(8) (S) vs. Frequency (IRG4BC20W), Rgate=33Ω, Vcc=15V

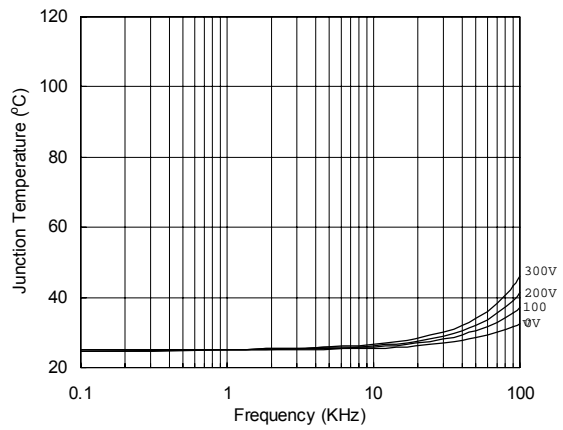


Figure 50. IR2136/IR21362(3)(5)(6)(7)(8) (S) vs. Frequency (IRG4BC30W), Rgate=15Ω, Vcc=15V

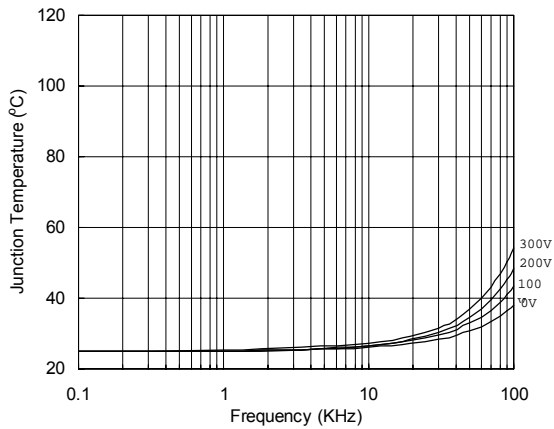


Figure 51. IR2136/IR21362(3)(5)(6)(7)(8) (S) vs. Frequency (IRG4BC40W), Rgate=10Ω, Vcc=15V

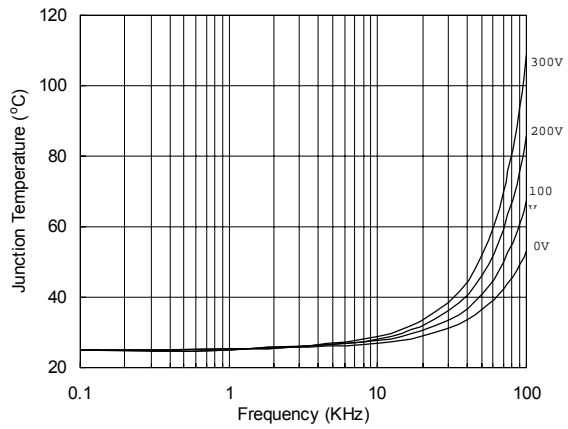
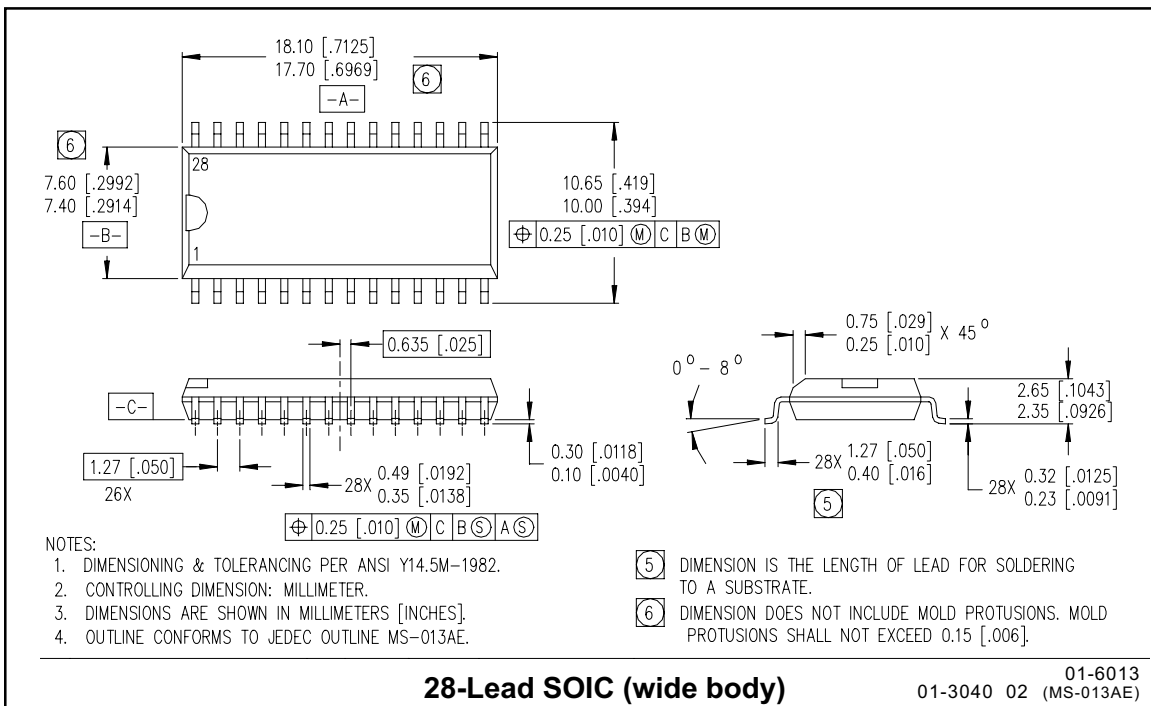
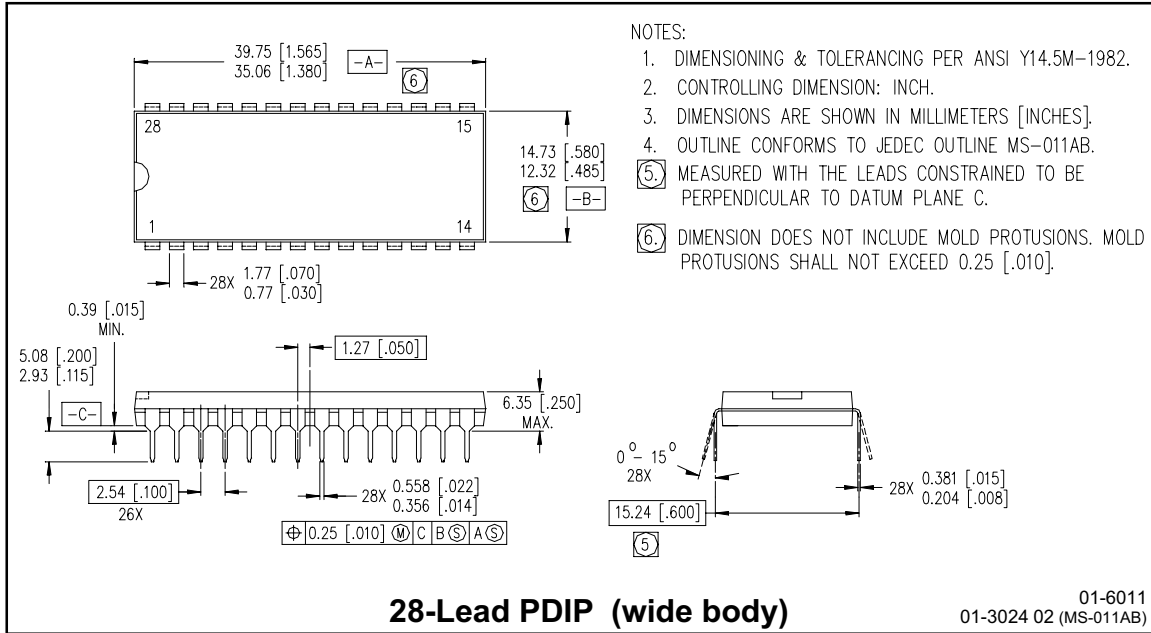


Figure 52. IR2136/IR21362(3)(5)(6)(7)(8) (S) vs. Frequency (IRG4PC50W), Rgate=5Ω, Vcc=15V

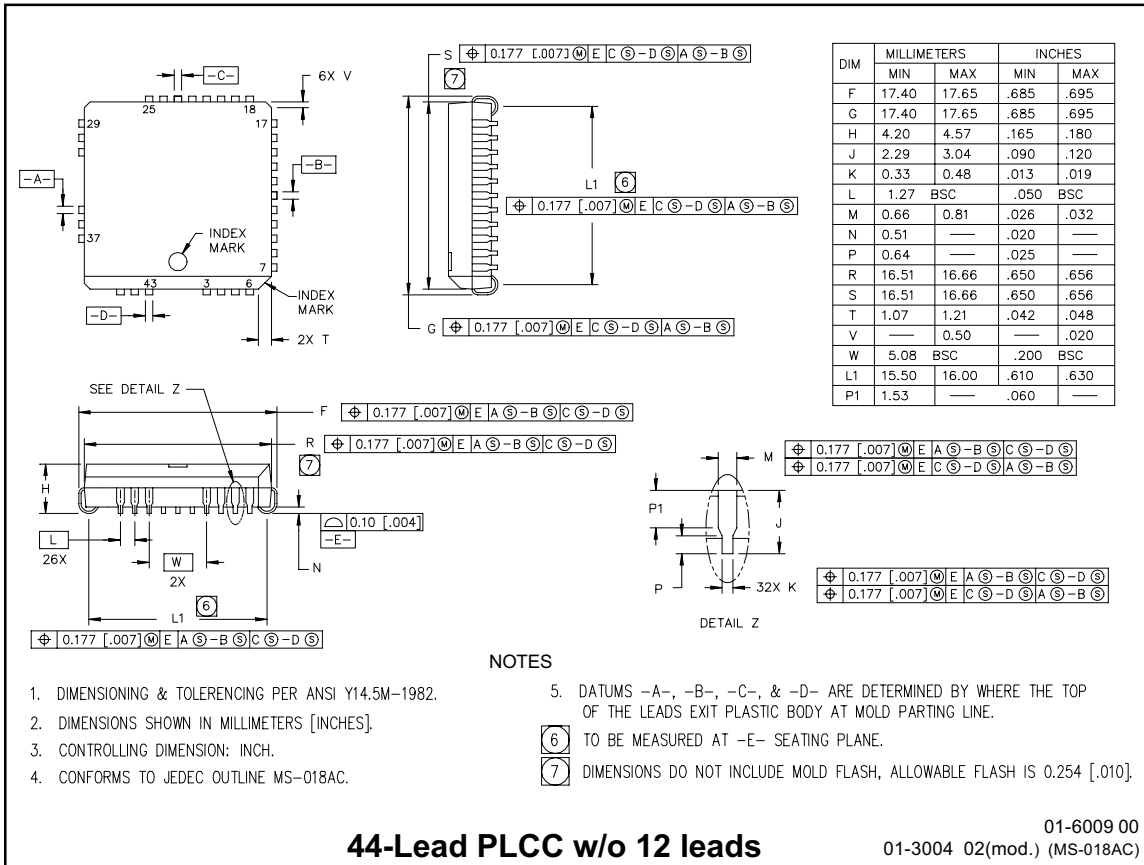
IR2136(2)(3)(5)(6)(7)(8)(J&S) & (PbF)

International
IR Rectifier

Case outlines



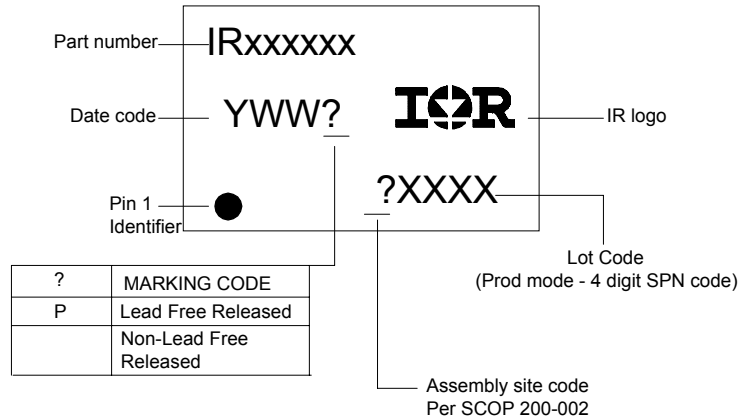
IR2136(2)(3)(5)(6)(7)(8)(J&S) & (PbF)



IR2136(2)(3)(5)(6)(7)(8)(J&S) & (PbF)

International
IR Rectifier

LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

Basic Part

28-Lead PDIP IR2136/IR21363(5)(6)(7)(8)	order IR2136/IR21363(5)(6)(7)(8)
28-Lead SOIC IR2136/IR21363(5)(6)(7)(8) (S)	order IR2136/IR21363(5)(6)(7)(8) (S)
44-Lead PLCC IR2136/IR21363(5)(6)(7)(8) (J)	order IR2136/IR21363(5)(6)(7)(8) (J)
28-Lead PDIP IR21362	order IR21362
28-Lead SOIC IR21362S	order IR21362S
44-Lead PLCC IR21362J	order IR21362J

Leadfree Part

28-Lead PDIP IR2136/IR21363(5)(6)(7)(8)	order IR2136/IR21363(5)(6)(7)(8)PbF
28-Lead SOIC IR2136/IR21363(5)(6)(7)(8) (S)	order IR2136/IR21363(5)(6)(7)(8) (S)PbF
44-Lead PLCC IR2136/IR21363(5)(6)(7)(8) (J)	order IR2136/IR21363(5)(6)(7)(8) (J)PbF
28-Lead PDIP IR21362	order IR21362PbF
28-Lead SOIC IR21362S	order IR21362SPbF
44-Lead PLCC IR21362J	order IR21362JPbF

International
IR Rectifier

WORLD HEADQUARTERS: 233 Kansas Street, El Segundo, California 90245 Tel: (310) 252-7105

This product has been qualified per industrial level
http://www.irf.com/ Data and specifications subject to change without notice. 5/25/2005